# DDR5 SDRAM-SODIMM

8GB based on 16Gbit (2Gx4) component

**Revision 1.0 (APR., 2026)**
-Initial Release

# 262-pin SODIMM DDR5 SDRAM

## 1. Features

- DDR5 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the DDR5 SODIMM core data sheet
- 262-pin, DDR5 unbuffered dual in-line memory module (DDR5 SODIMM)
- Fast data transfer rate: PC5-4800
- 8GB (1Gig x 64)
- Single-rank
- 16 internal banks; 4 groups of 4 banks each

## 2. Ordering Information

| Part Number | Density | Organization | Component Composition | # of Rank | Description |
|---|---|---|---|---|---|
| FD548S8GV | 8GB | 1Gx64 | 1Gx16 x 4pcs | 1 | PC5-4800 |

Note: Last character of the Part Number (x) represents DRAM vendor
S=Samsung; M=Micron; H=Hynix

## 3. Key Timing Parameters

| | DDR5-4800 | Unit |
|---|---|---|
| CL-tRCD-tRP | 40-39-39 | tCK |
| CAS Latency | 40 | tCK |

## 4. Address Configuration

| Organization | Row Address | Column Address | Bank Address | Bank Group Address | Module rank address |
|---|---|---|---|---|---|
| 1Gx16(16Gb) base | A0-A15 | A0-A9 | BA0-BA1 | BG0-BG1 | CS0_n |

## 5. DIMM Pin Descriptions

| Pin Name | Description | Pin Name | Description |
|---|---|---|---|
| CA0_A – CA12_A,<br>CA0_B – CA12_B | SDRAM<br>Command/Address bus | HSCL | SidebandBus clock |
| CS0_A_n – CS1_A_n,<br>CS0_B_n – CS1_B_n | SDRAM Chip Select | HSDA | SidebandBus data |
| DQ0_A – DQ31_A,<br>DQ0_B – DQ31_B | DIMM memory data bus | HSA | SidebandBus address |
| CB0_A – CB3_A,<br>CB0_B – CB3_B | DIMM ECC check bits | ALERT_n | SDRAM ALERT_n |
| DQS0_A_t –<br>DQS4_A_t,<br>DQS0_B_t –<br>DQS4_B_t | SDRAM data strobes<br>(positive line of<br>differential pair) | RESET n | Set DRAMs to a Known State |
| DQS0_A_c –<br>DQS4_A_c,<br>DQS0_B_c –<br>DQS4_B_c | SDRAM data strobes<br>(negative line of<br>differential pair) | VIN_BULK | 5 V power input supply to the<br>PMIC for analog circuits |
| DM0_A_n –<br>DM3_A_n,<br>DM0_B_n – DM3_B_n | SDRAM data masks | VSS | Power supply return (ground) |
| CK0_A_t, CK1_A_t,<br>CK0_B_t, CK1_B_t | SDRAM clocks (positive<br>line of differential pair) | PWR GOOD | Power good indicator |
| CK0_A_c, CK1_A_c,<br>CK0_B_c, CK1_B_c | SDRAM clocks (negative<br>line of differential pair) | PWR_EN | PMIC Enable |
| | | RFU | Reserved for future use |

NOTE 1 : DDR5 SODIMM has 2 channels (channel-A and channel-B) of signal bus. The signals with suffix: _A (e.g., DQ0_A) are for channel-A, and the signals with suffix: _B (e.g., DQ0_B) are for channel-B

## 6. Input/Output Functional Descriptions

| Symbol | Type | Function |
|---|---|---|
| CK0_A_t, CK0_A_c<br>CK1_A_t, CK1_A_c,<br>CK0_B_t, CK0_B_c<br>CK1_B_t, CK1_B_c | Input | Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c. |
| CA0_A - CA12_A,<br>CA0_B –CA12_B | Input | Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi cycle, the pins may not be interchanged between devices on the same bus. |
| CS0_A_n – CS1_A_n<br>CS0_B_n – CS1_B_n | Input | Chip Select: All commands are masked when CS_n is registered HIGH.<br>CS_n provides for external Rank selection on systems with multiple Ranks.<br>CS_n is considered part of the command code.<br>CS n is also used to enter and exit the parts from power down modes. |
| DQ0_A – DQ31_A<br>DQ0_B – DQ31_B | Input / Output | Data Input/Output: Bi-directio al data bus.<br>If CRC is enabled via Mode Register, then CRC code is added at the end of Data Burst. |

| Symbol | Type | Function |
|---|---|---|
| CB0_A – CB3_A<br>CB0_B – CB3_B | Input / Output | DIMM ECC check bits |
| DQS0_A_t – DQS4_A_t<br>DQS0_A_c – DQS4_A_c<br>DQS0_B_t – DQS4_B_t<br>DQS0_B_c – DQS4_B_c | Input / Output | Data Strobe: output with read data, input with write data.<br>Edge-aligned with read data, centered in write data.<br>DDR5 SDRAM supports differential data strobe only and does not support single-ended. |
| DM0_A_n – DM3_A_n<br>DM0_B_n – DM3_B_n | Input | Input Data Mask: DM_n is an input mask signal for write data.<br>Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS.<br>For x8 device, the function of DM_n is enabled by MR5:OP[5]=1. |
| ALERT_n | Input / Output | Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDDQ on board. |
| RESET_n | Input | Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ, |
| HSCL | Input | Host SidebandBus bus clock, supplied by the controller. |
| HSDA | Input / Output | Host SidebandBus data, connected from the controller to Hub or Host bus Target devices. |
| HSA | Input | Host SidebandBus bus device ID address pin; input to a Hub or other client device to distinguish between identical devices in the I3C-Basic address range. |
| RFU | | |
| PWR_GOOD | Open Drain | Power good indicator. Open Drain output.<br>The PMIC floats this pin high when VIN_Bulk input supply as well as all enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register.<br>The PMIC drives this pin low when VIN_Bulk input goes below the threshold or when any of the enabled switch output regulators exceed the threshold configured in the appropriate regis er or any LDO output regulator exceeds the threshold tolerance.<br>Input: The PMIC disabl s its output regulators when this pin is low. The LDO outputs shall remain on. |
| PWR_EN | Input | PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator.<br>This signal is connected to PMIC's VR_EN pin. |
| VIN_BULK | Supply | 5 V pow r input supply to the PMIC for analog circuits. |
| VSS | Supply | Ground |

## 7. Pin Assignmen

| Pin# | Front Side | Pin# | Back Side | Pin# | Front Side | Pin# | Back Side |
|---|---|---|---|---|---|---|---|
| 1 | VIN_BULK | 2 | HSA | 131 | CK0_A_t | 132 | CK1_A_t |
| 3 | VIN_BULK | 4 | HSCL | 133 | CK0_A_c | 134 | CK1_A_c |
| 5 | RFU | 6 | HSDA | 135 | VSS | 136 | VSS |
| 7 | PWR_GOOD | 8 | PWR_EN | 137 | CK0_B_t | 138 | CK1_B_t |
| 9 | VSS | 10 | VSS | 139 | CK0_B_c | 140 | CK1_B_c |
| 11 | DQ0_A | 12 | DQ1_A | 141 | VSS | 142 | VSS |
| 13 | VSS | 14 | VSS | 143 | RFU | 144 | CA12_B |
| 15 | DQ2_A | 16 | DQ3_A | 145 | CA11_B | 146 | CA10_B |
| 17 | VSS | 18 | VSS | 147 | VSS | 148 | VSS |
| 19 | DM0_A_n | 20 | DQS0_A_c | 149 | CA9_B | 150 | CA8_B |
| 21 | VSS | 22 | DQS0_A_t | 151 | CA7_B | 152 | CA6_B |
| 23 | DQ4_A | 24 | VSS | 153 | VSS | 154 | VSS |
| 25 | VSS | 26 | DQ5_A | 155 | CA5_B | 156 | CA4_B |
| 27 | DQ6_A | 28 | VSS | 157 | CA3_B | 158 | CA2_B |
| 29 | VSS | 30 | DQ7_A | 159 | VSS | 160 | VSS |
| 31 | DQ8_A | 32 | VSS | 161 | CS0_B_n | 162 | CA1_B |
| 33 | VSS | 34 | DQ09_A | 163 | RESET_n | 164 | CA0_B |
| 35 | DQ10_A | 36 | VSS | 165 | CS1_B_n | 166 | VSS |
| 37 | VSS | 38 | DQ11_A | 167 | VSS | 168 | CB0_B |
| 39 | DQS1_A_c | 40 | VSS | 169 | DQS4_B_c | 170 | VSS |
| 41 | DQS1_A_t | 42 | DM1_A_n | 171 | DQS4_B_t | 172 | CB1_B |
| 43 | VSS | 44 | VSS | 173 | VSS | 174 | VSS |
| 45 | DQ12_A | 46 | DQ13_A | 175 | CB3_B | 176 | CB2_B |
| 47 | VSS | 48 | VSS | 177 | VSS | 178 | VSS |
| 49 | DQ14_A | 50 | DQ15_A | 179 | DQ0_B | 180 | DQ1_B |
| 51 | VSS | 52 | VSS | 181 | VSS | 182 | VSS |
| 53 | DQ16_A | 54 | DQ17_A | 183 | DQ2_B | 184 | DQ3_B |
| 55 | VSS | 56 | VSS | 185 | VSS | 186 | VSS |
| 57 | DQ18_A | 58 | DQ19_A | 187 | DM0_B_n | 188 | DQS0_B_c |
| 59 | VSS | 60 | VSS | 189 | VSS | 190 | DQS0_B_t |
| 61 | DM2_A_n | 62 | DQS2_A_c | 191 | DQ4_B | 192 | VSS |
| 63 | VSS | 64 | DQS2_A_t | 193 | VSS | 194 | DQ5_B |
| 65 | DQ20_A | 66 | VSS | 195 | DQ6_B | 196 | VSS |
| 67 | VSS | 68 | DQ21_A | 197 | VSS | 198 | DQ7_B |
| 69 | DQ22_A | 70 | VSS | 199 | DQ8_B | 200 | VSS |

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|---|---|---|---|---|---|---|---|
| 71 | VSS | 72 | DQ23_A | 201 | VSS | 202 | DQ9_B |
| 73 | DQ24_A | 74 | VSS | 203 | DQ10_B | 204 | VSS |
| 75 | VSS | 76 | DQ25_A | 205 | VSS | 206 | DQ11_B |
| 77 | DQ26_A | 78 | VSS | 207 | DQS1_B_c | 208 | VSS |
| 79 | VSS | 80 | DQ27_A | 209 | DQS1_B_t | 210 | DM1_B_n |
| 81 | DQS3_A_c | 82 | VSS | 211 | VSS | 212 | VSS |
| 83 | DQS3_A_t | 84 | DM3_A_n | 213 | DQ12_B | 214 | DQ13_B |
| 85 | VSS | 86 | VSS | 215 | VSS | 216 | VSS |
| 87 | DQ28_A | 88 | DQ29_A | 217 | DQ14_B | 218 | DQ15_B |
| 89 | VSS | 90 | VSS | 219 | VSS | 220 | VSS |
| 91 | DQ30_A | 92 | DQ31_A | 221 | DQ16_B | 222 | DQ17_B |
| 93 | VSS | 94 | VSS | 223 | VSS | 224 | VSS |
| 95 | CB0_A | 96 | CB1_A | 225 | DQ18_B | 226 | DQ19_B |
| 97 | VSS | 98 | VSS | 227 | VSS | 228 | VSS |
| 99 | CB2_A | 100 | DQS4_A_c | 229 | DM2_B_n | 230 | DQS2_B_c |
| 101 | VSS | 102 | DQS4_A_t | 231 | VSS | 232 | DQS2_B_t |
| 103 | CB3_A | 104 | VSS | 233 | DQ20_B | 234 | VSS |
| 105 | VSS | 106 | CS0_A_n | 235 | VSS | 236 | DQ21_B |
| 107 | CA0_A | 108 | ALERT_n | 237 | DQ22_B | 238 | VSS |
| 109 | CA1_A | 110 | CS1_A_n | 239 | VSS | 240 | DQ23_B |
| 111 | VSS | 112 | VSS | 241 | DQ24_B | 242 | VSS |
| 113 | CA2_A | 114 | CA3_A | 243 | VSS | 244 | DQ25_B |
| 115 | CA4_A | 116 | CA5_A | 245 | DQ26_B | 246 | VSS |
| 117 | VSS | 118 | VSS | 247 | VSS | 248 | DQ27_B |
| 119 | CA6_A | 120 | CA7_A | 249 | DQS3_B_c | 250 | VSS |
| 121 | CA8_A | 122 | CA9_A | 251 | DQS3_B_t | 252 | DM3_B_n |
| 123 | VSS | 124 | VSS | 253 | VSS | 254 | VSS |
| 125 | CA10_A | 126 | CA11_A | 255 | DQ28_B | 256 | DQ29_B |
| KEY | | | | 257 | VSS | 258 | VSS |
| 127 | CA12_A | 128 | RFU | 259 | DQ30_B | 260 | DQ31_B |
| 129 | VSS | 130 | VSS | 261 | VSS | 262 | VSS |

## 8. Absolute Maximum DC Ratings

| Symbol | Parameter | Rating | Units | NOTE |
|---|---|---|---|---|
| VDD | Voltage on VDD pin relative to Vss | -0.3 ~ 1.4 | V | 1,3 |
| VDDQ | Voltage on VDDQ pin relative to Vss | -0.3 ~ 1.4 | V | 1,3 |
| VPP | Voltage on VPP pin relative to Vss | -0.3 ~ 2.1 | V | 4 |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to Vss | -0.3 ~ 1.4 | V | 1,3,5 |
| $T_{STG}$ | Storage Temperature | -55 to +100 | ℃ | 1,2 |

NOTE 1 Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

NOTE 2 Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

NOTE 3 VDD and VDDQ must be within 300 mV of each other at all times. When VDD and VDDQ are less than 500 mV

NOTE 4 VPP must be equal or greater than VDD/VDDQ at all times.

NOTE 5 Overshoot area above 1.5 V is specified in Section 8.3.4, Section 8.3.5, and Section 8.3.6.

## 9. DRAM Component Operating Temperature Range

| Symbol | Parameter | Rating | Units | NOTE |
|---|---|---|---|---|
| $T_{OPER}$ | Normal Operating Temperature Range | 0 to 85 | ºC | 1,2,3 |
| | Extended Temperature Range | 85 to 95 | ºC | 1,2,3,4 |

NOTE 1 Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement condi-tions, please refer to JESD51-2 standard.

NOTE 2 The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85°C under all operating conditions.

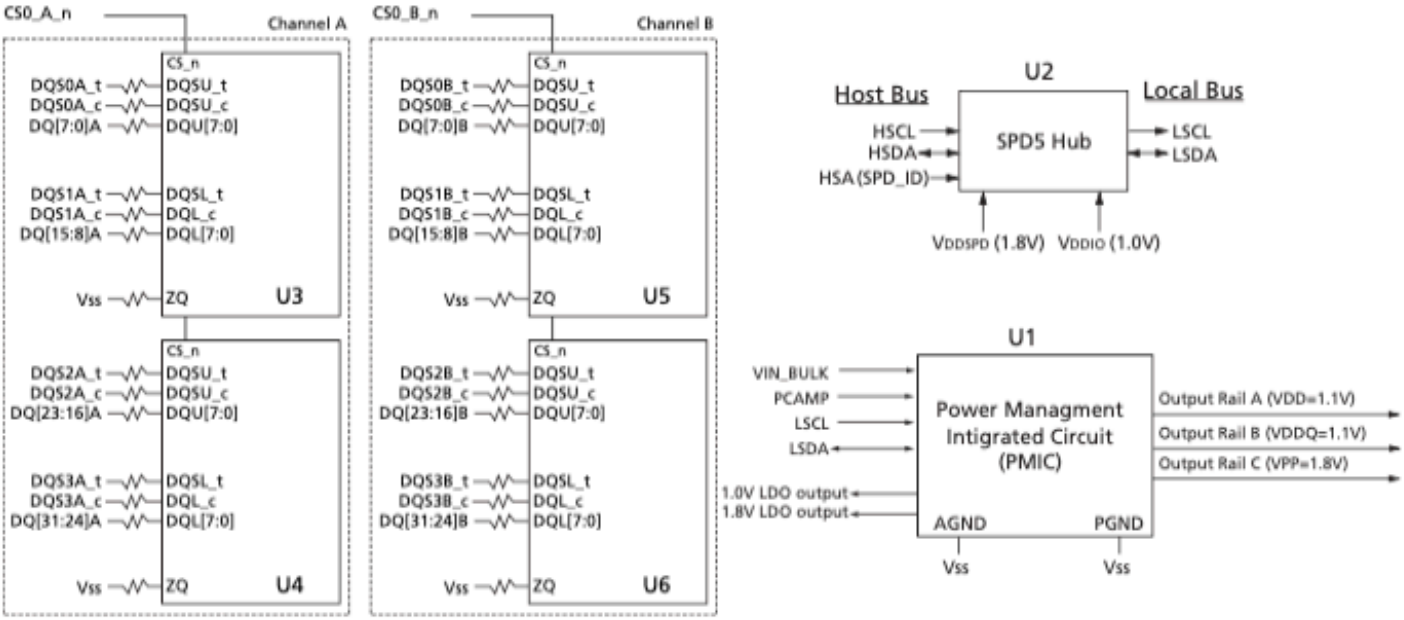
NOTE 3 Operating Temperature for 3DS needs to be derated by the number of DRAM dies as: [$T_{OPER}$ – (2.5°C × $\log_2$N)], where N is the number of the stacked dies.

NOTE 4 Some applica**tio**ns require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are supported in this range, but the following additional conditions apply:

a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9us. It is also possible to specify a component with 1X refresh (tREFI to 7.8us) in the Extended Temperature Range. Please refer to supplier's datasheet and/or the DIMM SPD for option availability.

b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6=0b and MR2 A7=1b) or enable the optional Auto Self-Refresh mode (MR2 A6=1b and MR2 A7=0b). Please refer to the supplier's datasheet and/or the DIMM SPD for Auto Self-Refresh option availability. Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

## 10. Functional Block Diagram:




Notes: 1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

2. Functional block diagram is for reference only.

## 11. AC&DC Operating Conditions

Recommended operating conditions (Voltage referred to Vss=0V, TA=0 to 70°C)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Device Supply Voltage | 1.067 | 1.1 | 1.166 | V |
| $V_{DDQ}$ | Supply Voltage for I/O | 1.067 | 1.1 | 1.166 | V |
| $V_{PP}$ | Core Power Voltage | 1.746 | 1.8 | 1.908 | V |

## 12. Physical Dimensions: