DDR5 SDRAM

UnBuffered DIMM

8GB based on 16Gbit (2Gx4) component

Revision 1.0 (APR., 2026)
-Initial Release

288-pin UDIMM DDR5 SDRAM

1. Features

- DDR5 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the DDR5 UDIMM core data sheet
- 288-pin, DDR5 unbuffered dual in-line memory module (DDR5 UDIMM)
- Fast data transfer rate: PC5-5600
- 8GB (1Gig x 64)
- Single-rank
- 16 internal banks; 4 groups of 4 banks each

2. Ordering Information

Part Number	Density	Organization	Component Composition	# of Rank	Description
FD556U8GV	8GB	1Gbx64	1Gx16 x 4pcs	1	PC5-5600

Note: Last character of the Part Number (x) represents DRAM vendor
S=Samsung; M=Micron; H=Hynix

3. Key Timing Parameters

	DDR5-5600	Unit
CL-tRCD-tRP	46-45-45	tCK
CAS Latency	46	tCK

4. Address Configuration

Organization	Row Address	Column Address	Bank Address	Bank Group Address	Module rank address
1Gx16(16Gb) base	A0-A15	A0-A9	BA0-BA1	BG0-BG1	CS0_n

5. DIMM Pin Descriptions

Pin Name	Description	Pin Name	Description
CA0_A – CA12_A, CA0_B – CA12_B	SDRAM Command/Address bus	HSCL	SidebandBus clock
CS0_A_n – CS1_A_n, CS0_B_n – CS1_B_n	SDRAM Chip Select	HSDA	SidebandBus data
DQ0_A – DQ31_A, DQ0_B – DQ31_B	DIMM memory data bus	HSA	SidebandBus address
CB0_A – CB3_A, CB0_B – CB3_B	DIMM ECC check bits	ALERT_n	SDRAM ALERT_n
DQS0_A_t – DQS4_A_t, DQS0_B_t – DQS4_B_t	SDRAM data strobes (positive line of differential pair)	RESET n	Set DRAMs to a Known State
DQS0_A_c – DQS4_A_c, DQS0_B_c – DQS4_B_c	SDRAM data strobes (negative line of differential pair)	VIN_BULK	5 V power input supply to the PMIC for analog circuits
DM0_A_n – DM3_A_n, DM0_B_n – DM3_B_n	SDRAM data masks	VSS	Power supply return (ground)
CK0_A_t, CK1_A_t, CK0_B_t, CK1_B_t	SDRAM clocks (positive line of differential pair)	PWR GOOD	Power good indicator
CK0_A_c, CK1_A_c, CK0_B_c, CK1_B_c	SDRAM clocks (negative line of differential pair)	PWR_EN	PMIC Enable
		RFU	Reserved for future use

NOTE 1 : DDR5 UDIMM has 2 channels (channel-A and channel-B) of signal bus. The signals with suffix: _A (e.g., DQ0_A) are for channel-A, and the signals with suffix: _B (e.g., DQ0_B) are for channel-B

6. Input/Output Functional Descriptions

Symbol	Type	Function
CK0_A_t, CK0_A_c CK1_A_t, CK1_A_c, CK0_B_t, CK0_B_c CK1_B_t, CK1_B_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA0_A - CA12_A, CA0_B –CA12_B	Input	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi cycle, the pins may not be interchanged between devices on the same bus.
CS0_A_n – CS1_A_n CS0_B_n – CS1_B_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS n is also used to enter and exit the parts from power down modes.
DQ0_A – DQ31_A DQ0_B – DQ31_B	Input / Output	Data Input/Output: Bi-directio al data bus. If CRC is enabled via Mode Register, then CRC code is added at the end of Data Burst.

Symbol	Type	Function
CB0_A – CB3_A CB0_B – CB3_B	Input / Output	DIMM ECC check bits
DQS0_A_t – DQS4_A_t DQS0_A_c – DQS4_A_c DQS0_B_t – DQS4_B_t DQS0_B_c – DQS4_B_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
DM0_A_n – DM3_A_n DM0_B_n – DM3_B_n	Input	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1.
ALERT_n	Input / Output	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDDQ on board.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ,
HSCL	Input	Host SidebandBus bus clock, supplied by the controller.
HSDA	Input / Output	Host SidebandBus data, connected from the controller to Hub or Host bus Target devices.
HSA	Input	Host SidebandBus bus device ID address pin; input to a Hub or other client device to distinguish between identical devices in the I3C-Basic address range.
RFU		
PWR_GOOD	Open Drain	Power good indicator. Open Drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as all enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or when any of the enabled switch output regulators exceed the threshold configured in the appropriate regis er or any LDO output regulator exceeds the threshold tolerance. Input: The PMIC disabl s its output regulators when this pin is low. The LDO outputs shall remain on.
PWR_EN	Input	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This signal is connected to PMIC's VR_EN pin.
VIN_BULK	Supply	5 V pow r input supply to the PMIC for analog circuits.
VSS	Supply	Ground

7. Pin Assignmen

Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	VIN_BULK	145	VIN_BULK	75	RFU	219	RFU
2	RFU	146	VIN_BULK	KEY			
3	RFU	147	PWR_GOOD	76	RFU	220	RFU
4	HSCL	148	HSA	77	VSS	221	VSS
5	HSDA	149	RFU	78	CK0_B_t	222	CK1_B_t
6	VSS	150	VSS	79	CK0_B_c	223	CK1_B_c
7	RFU	151	PWR_EN	80	VSS	224	VSS
8	VSS	152	RFU	81	RFU	225	RFU
9	DQ0_A	153	VSS	82	CA12_B	226	RFU
10	VSS	154	DQ2_A	83	VSS	227	VSS
11	DQ1_A	155	VSS	84	CA10_B	228	CA11_B
12	VSS	156	DQ3_A	85	CA8_B	229	CA9_B
13	DQS0_A_c	157	VSS	86	VSS	230	VSS
14	DQS0_A_t	158	DM0_A_n	87	CA6_B	231	CA7_B
15	VSS	159	VSS	88	CA4_B	232	CA5_B
16	DQ4_A	160	DQ6_A	89	VSS	233	VSS
17	VSS	161	VSS	90	CA2_B	234	CA3_B

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Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
18	DQ5_A	162	DQ7_A	91	CA0_B	235	CA1_B
19	VSS	163	VSS	92	VSS	236	VSS
20	DQ8_A	164	DQ10_A	93	CS0_B_n	237	CS1_B_n
21	VSS	165	VSS	94	VSS	238	VSS
22	DQ9_A	166	DQ11_A	95	RESET_n	239	DQS4_B_c
23	VSS	167	VSS	96	VSS	240	DQS4_B_t
24	DM1_A_n	168	DQS1_A_c	97	CB0_B	241	VSS
25	VSS	169	DQS1 A t	98	VSS	242	CB2_B
26	DQ12_A	170	VSS	99	CB1_B	243	VSS
27	VSS	171	DQ14 A	100	VSS	244	CB3_B
28	DQ13_A	172	VSS	101	DQ0_B	245	VSS
29	VSS	173	DQ15 A	102	VSS	246	DQ2_B
30	DQ16_A	174	VSS	103	DQ1_B	247	VSS
31	VSS	175	DQ18 A	104	VSS	248	DQ3_B
32	DQ17_A	176	VSS	105	DQS0_B_c	249	VSS
33	VSS	177	DQ19 A	106	DQS0_B_t	250	DM0_B_n
34	DQS2_A_c	178	VSS	107	VSS	251	VSS

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Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
35	DQS2_A_t	179	DM2 A n	108	DQ4_B	252	DQ6_B
36	VSS	180	VSS	109	VSS	253	VSS
37	DQ20_A	181	DQ22_A	110	DQ5_B	254	DQ7_B
38	VSS	182	VSS	111	VSS	255	VSS
39	DQ21_A	183	DQ23_A	112	DQ8_B	256	DQ10_B
40	VSS	184	VSS	113	VSS	257	VSS
41	DQ24_A	185	DQ26_A	114	DQ9_B	258	DQ11_B
42	VSS	186	VSS	115	VSS	259	VSS
43	DQ25_A	187	DQ27_A	116	DM1_B_n	260	DQS1_B_c
44	VSS	188	VSS	117	VSS	261	DQS1_B_t
45	DM3_A_n	189	DQS3_A_c	118	DQ12_B	262	VSS
46	VSS	190	DQS3_A_t	119	VSS	263	DQ14_B
47	DQ28_A	191	VSS	120	DQ13_B	264	VSS
48	VSS	192	DQ30_A	121	VSS	265	DQ15_B
49	DQ29_A	193	VSS	122	DQ16_B	266	VSS
50	VSS	194	DQ31_A	123	VSS	267	DQ18_B
51	CB0_A	195	VSS	124	DQ17_B	268	VSS

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Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
52	VSS	196	CB2_A	125	VSS	269	DQ19_B
53	CB1_A	197	VSS	126	DQS2_B_c	270	VSS
54	VSS	198	CB3_A	127	DQS2_B_t	271	DM2_B_n
55	DQS4_A_c	199	VSS	128	VSS	272	VSS
56	DQS4_A_t	200	ALERT_n	129	DQ20_B	273	DQ22_B
57	VSS	201	VSS	130	VSS	274	VSS
58	CS0_A_n	202	CS1_A_n	131	DQ21_B	275	DQ23_B
59	VSS	203	VSS	132	VSS	276	VSS
60	CA0_A	204	CA1_A	133	DQ24_B	277	DQ26_B
61	CA2_A	205	CA3_A	134	VSS	278	VSS
62	VSS	206	VSS	135	DQ25_B	279	DQ27_B
63	CA4_A	207	CA5_A	136	VSS	280	VSS
64	CA6_A	208	CA7 A	137	DM3_B_n	281	DQS3_B_c
65	VSS	209	VSS	138	VSS	282	DQS3_B_t
66	CA8_A	210	CA9 A	139	DQ28_B	283	VSS

Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
67	CA10_A	211	CA11 A	140	VSS	284	DQ30_B
68	VSS	212	VSS	141	DQ29_B	285	VSS
69	CA12_A	213	RFU	142	VSS	286	DQ31_B
70	RFU	214	RFU	143	RFU	287	VSS
71	VSS	215	VSS	144	RFU	288	RFU
72	CK0_A_t	216	CK1 A t				
73	CK0_A_c	217	CK1 A c				
74	VSS	218	VSS				

8. Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.4	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.4	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 2.1	V	4
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.3 ~ 1.4	V	1,3,5
T_{STG}	Storage Temperature	-55 to +100	℃	1,2

NOTE 1 Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

NOTE 2 Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

NOTE 3 VDD and VDDQ must be within 300 mV of each other at all times. When VDD and VDDQ are less than 500 mV

NOTE 4 VPP must be equal or greater than VDD/VDDQ at all times.

NOTE 5 Overshoot area above 1.5 V is specified in Section 8.3.4, Section 8.3.5, and Section 8.3.6.

9. DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	NOTE
T_{OPER}	Normal Operating Temperature Range	0 to 85	ºC	1,2,3
	Extended Temperature Range	85 to 95	ºC	1,2,3,4

NOTE 1 Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement condi-tions, please refer to JESD51-2 standard.

NOTE 2 The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85°C under all operating conditions.

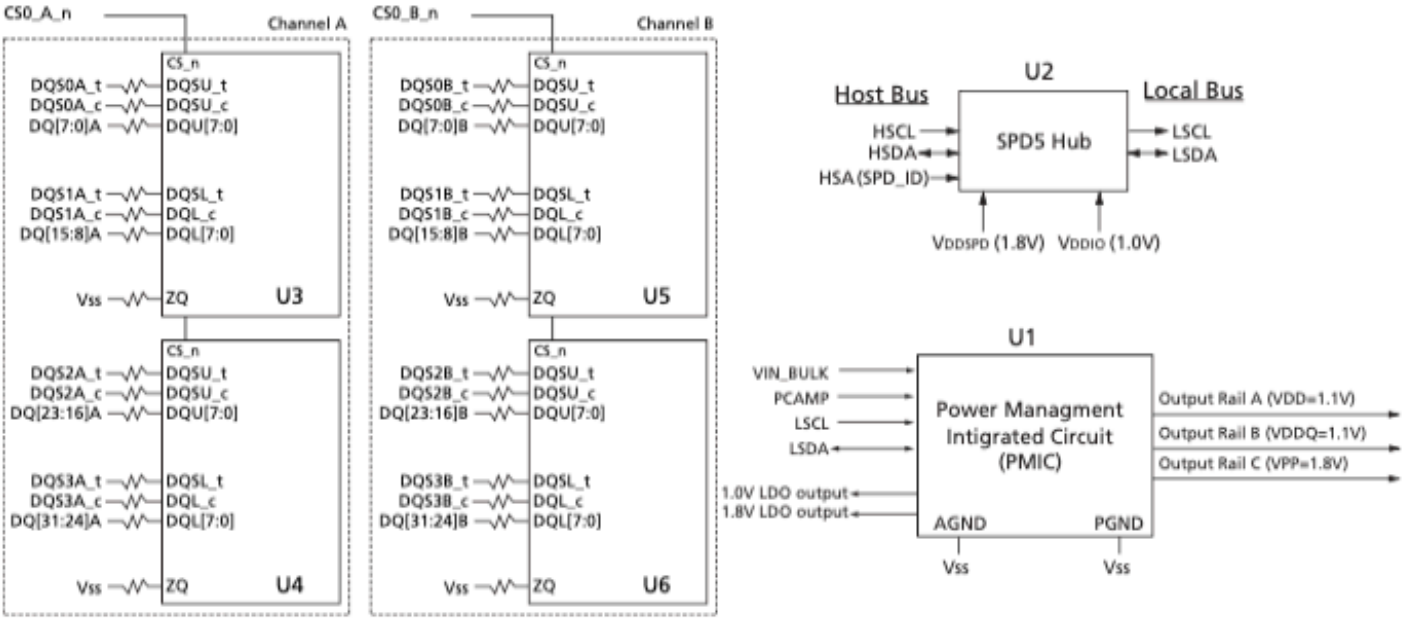
NOTE 3 Operating Temperature for 3DS needs to be derated by the number of DRAM dies as: [T_{OPER} – (2.5°C × $\log_2$N)], where N is the number of the stacked dies.

NOTE 4 Some applica**tio**ns require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are supported in this range, but the following additional conditions apply:

a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9us. It is also possible to specify a component with 1X refresh (tREFI to 7.8us) in the Extended Temperature Range. Please refer to supplier's datasheet and/or the DIMM SPD for option availability.

b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6=0b and MR2 A7=1b) or enable the optional Auto Self-Refresh mode (MR2 A6=1b and MR2 A7=0b). Please refer to the supplier's datasheet and/or the DIMM SPD for Auto Self-Refresh option availability. Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

10. Functional Block Diagram:



Notes: 1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

2. Functional block diagram is for reference only.

11. AC&DC Operating Conditions

Recommended operating conditions (Voltage referred to Vss=0V, TA=0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Device Supply Voltage	1.067	1.1	1.166	V
V_{DDQ}	Supply Voltage for I/O	1.067	1.1	1.166	V
V_{PP}	Core Power Voltage	1.746	1.8	1.908	V

12. Physical Dimensions: