

DDR2 Unbuffered DIMM Module

2GB based on 1Gbit components

60 Balls TFBGA with Pb-Free



Revision 1.0 (Mar. 2006)
-Initial Release

1.0 Feature

- JEDEC standard 1.8V +/- 0.1V Power Supply
- Standard Double-Data-Rate-Two Synchronous DRAMs with single 1.8V power supply
- Programmable CAS latencies (3,4,5,6), Burst Length (4 & 8) and Burst Type
- Auto Refresh (CRB) and Self Refresh
- Bi-directional Differential Data Strobe (Single ended data strobe is option)
- Off Chip Driver (OCD) impedance adjustment
- On-Die termination with selectable values (50/75/150 ohms or disable)
- PASR (Partial Array Self Refresh)
- Average Refresh Period 7.8us at lower than a TCASE 85°C, 3.9us at 85°C < TCASE < 95 °C - support High Temperature Self-Refresh rate enable feature
- Serial presence detect with EEPROM
- DIMM Dimension (Nominal) 30.00 mm high, 133.35 mm wide
- All speed grades faster than DDR400 comply with DDR400 timing specifications
- Based on JEDEC standard reference Raw Cards Lay out.
- RoHS compliant
- Gold plated contacts

2.0 Ordering Information

Part number	Density	Module Organization	Component composition	Component PKG	Module Rank	Description
T800UB2GV	2GB	256Mx64	128Mx8*16	TFBGA	2	2GB 2Rx8 PC2-6400R

3.0 Operating Frequencies

	DDR2-800	Unit
Speed @ CL6	800	Mbps
CL-tRCD-tRP	6-6-6	CK

4.0 Absolute Maximum DC Rating

Symbol	Parameter	Rating	Units
V _{in} , V _{out}	Voltage on any pin relative to V _{SS}	-0.5 ~ 2.3	V
V _{DD}	Voltage on V _{DD} & V _{DDQ} supply relative to V _{SS}	-1.0 ~ 2.3	V
V _{DDQ}	Short circuit current	-0.5 ~ 2.3	V
V _{DDL}	Power dissipation	-0.5 ~ 2.3	V
T _{STG}	Storage Temperature	-55 ~ + 100	°C

240-Pin Unbuffered DIMM

DDR2 SDRAM

5.0 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V _{REF}	121	V _{SS}	31	DQ19	151	V _{SS}	61	A4	181	V _{DDQ}	91	V _{SS}	211	DM5/DQS14
2	V _{SS}	122	DQ4	32	V _{SS}	152	DQ28	62	V _{DDQ}	182	A3	92	$\overline{\text{DQS5}}$	212	NC/ $\overline{\text{DQS14}}$
3	DQ0	123	DQ5	33	DQ24	153	DQ29	63	A2	183	A1	93	DQS5	213	V _{SS}
4	DQ1	124	V _{SS}	34	DQ25	154	V _{SS}	64	V _{DD}	184	V _{DD}	94	V _{SS}	214	DQ46
5	V _{SS}	125	DM0/DQS9	35	V _{SS}	155	DM3/DQS12	KEY				95	DQ42	215	DQ47
6	$\overline{\text{DQS0}}$	126	NC/ $\overline{\text{DQS9}}$	36	$\overline{\text{DQS3}}$	156	NC/ $\overline{\text{DQS12}}$	65	V _{SS}	185	CK0	96	DQ43	216	V _{SS}
7	DQS0	127	V _{SS}	37	DQS3	157	V _{SS}	66	V _{SS}	186	$\overline{\text{CK0}}$	97	V _{SS}	217	DQ52
8	V _{SS}	128	DQ6	38	V _{SS}	158	DQ30	67	V _{DD}	187	V _{DD}	98	DQ48	218	DQ53
9	DQ2	129	DQ7	39	DQ26	159	DQ31	68	NC/Par_in	188	A0	99	DQ99	219	V _{SS}
10	DQ3	130	V _{SS}	40	DQ27	160	V _{SS}	69	V _{DD}	189	V _{DD}	100	VSS	220	RFU
11	V _{SS}	131	DQ12	41	V _{SS}	161	CB4	70	A10/AP	190	BA1	101	SA2	221	RFU
12	DQ8	132	DQ13	42	CB0	162	CB5	71	BA0	191	V _{DDQ}	102	NC(Test)	222	V _{SS}
13	DQ9	133	V _{SS}	43	CB1	163	V _{SS}	72	V _{DDQ}	192	$\overline{\text{RAS}}$	103	V _{SS}	223	DM6/DQS15
14	V _{SS}	134	DM1/DQS10	44	V _{SS}	164	DM8/DQS17	73	$\overline{\text{WE}}$	193	S0	104	$\overline{\text{DQS6}}$	224	NC/ $\overline{\text{DQS15}}$
15	$\overline{\text{DQS1}}$	135	NC/ $\overline{\text{DQS10}}$	45	$\overline{\text{DQS8}}$	165	NC/ $\overline{\text{DQS17}}$	74	$\overline{\text{CAS}}$	194	V _{DDQ}	105	DQS6	225	V _{SS}
16	DQS1	136	V _{SS}	46	DQS8	166	V _{SS}	75	VDDQ	195	ODT0	106	V _{SS}	226	DQ54
17	V _{SS}	137	RFU	47	V _{SS}	167	CB6	76	S1	196	A13	107	DQ50	227	DQ55
18	$\overline{\text{RESET}}$	138	RFU	48	CB2	168	CB7	77	ODT1	197	V _{DD}	108	DQ51	228	V _{SS}
19	NC	139	V _{SS}	49	CB3	169	V _{SS}	78	V _{DDQ}	198	V _{SS}	109	V _{SS}	229	DQ60
20	V _{SS}	140	DQ14	50	V _{SS}	170	V _{DDQ}	79	V _{SS}	199	DQ36	110	DQ56	230	DQ61
21	DQ10	141	DQ15	51	V _{DDQ}	171	CKE1	80	DQ32	200	DQ37	111	DQ57	231	V _{SS}
22	DQ11	142	VSS	52	CKE0	172	V _{DD}	81	DQ33	201	V _{SS}	112	V _{SS}	232	DM7/DQS16
23	V _{SS}	143	DQ20	53	V _{DD}	173	NC	82	V _{SS}	202	DM4/DQS13	113	$\overline{\text{DQS7}}$	233	NC/ $\overline{\text{DQS16}}$
24	DQ16	144	DQ21	54	NC	174	NC	83	$\overline{\text{DQS4}}$	203	NC/ $\overline{\text{DQS13}}$	114	DQS7	234	V _{SS}
25	DQ17	145	V _{SS}	55	NC/Err_Out	175	V _{DDQ}	84	DQS4	204	V _{SS}	115	V _{SS}	235	DQ62
26	V _{SS}	146	DM2/DQS11	56	V _{DDQ}	176	A12	85	V _{SS}	205	DQ38	116	DQ58	236	DQ63
27	$\overline{\text{DQS2}}$	147	NC/ $\overline{\text{DQS11}}$	57	A11	177	A9	86	DQ34	206	DQ39	117	DQ59	237	V _{SS}
28	DQS2	148	V _{SS}	58	A7	178	V _{DD}	87	DQ35	207	V _{SS}	118	VSS	238	V _{DD} SPD
29	V _{SS}	149	DQ22	59	V _{DD}	179	A8	88	V _{SS}	208	DQ44	119	SDA	239	SA0
30	DQ18	150	DQ23	60	A5	180	A6	89	DQ40	209	DQ45	120	SCL	240	SA1
								90	DQ41	210	V _{SS}				

NC = No Connect, RFU = Reserved for Future Use

1. Pin196(A13) is used for x4/x8 base Unbuffered DIMM.

2. The TEST pin is reserved for bus analysis tools and is not connected on standard memory module products (DIMMs.)

6.0 DIMM Pin Description

Pin Name	Function	Pin Name	Function
A0 ~ A9, A11~A13	Address input (Multiplexed)	ODT0~ODT1	On Die Termination
A10/AP	Address Input/Auto pre-charge	CB0~CB7	Data check bits Input/Output
BA0 ~ BA1	Bank Select	DQ0~DQ63	Data Input/Output
CK0 ~ CK2	Clock (positive line of different pair)	$\overline{\text{DQS0}}\sim\overline{\text{DQS8}}$	Data strobes, negative line
$\overline{\text{CK0}}\sim\overline{\text{CK2}}$	Clock (negative line of different pair)	DM(0~8), DQS(9~17)	Data Masks/Data strobes (Read)
CKE0, CKE1	Clock enable input	$\overline{\text{DQS9}}\sim\overline{\text{DQS17}}$	Data strobes (Read), negative line
$\overline{\text{S0}}, \overline{\text{S1}}$	Chip select input	DQS0~DQS8	Data Strobes
$\overline{\text{RAS}}$	Row address strobe	RFU	Reserved for future used
$\overline{\text{CAS}}$	Column address strobe	NC	No connection
$\overline{\text{WE}}$	Write Enable	TEST	Memory bus test tool
SCL	SPD Clock Input	V _{DD}	Core Power
SDA	SPD Data Input/Output	V _{DDQ}	I/O Power
SA0~SA2	SPD Address	V _{SS}	Ground
Par_In	Parity bit for address & Control bus	V _{REF}	Input/Output Reference
Err_Out	Parity error found in the Address and Control bus	V _{DDSPD}	Serial EEPROM positive power supply
$\overline{\text{RESET}}$	Register and PLL control pin		

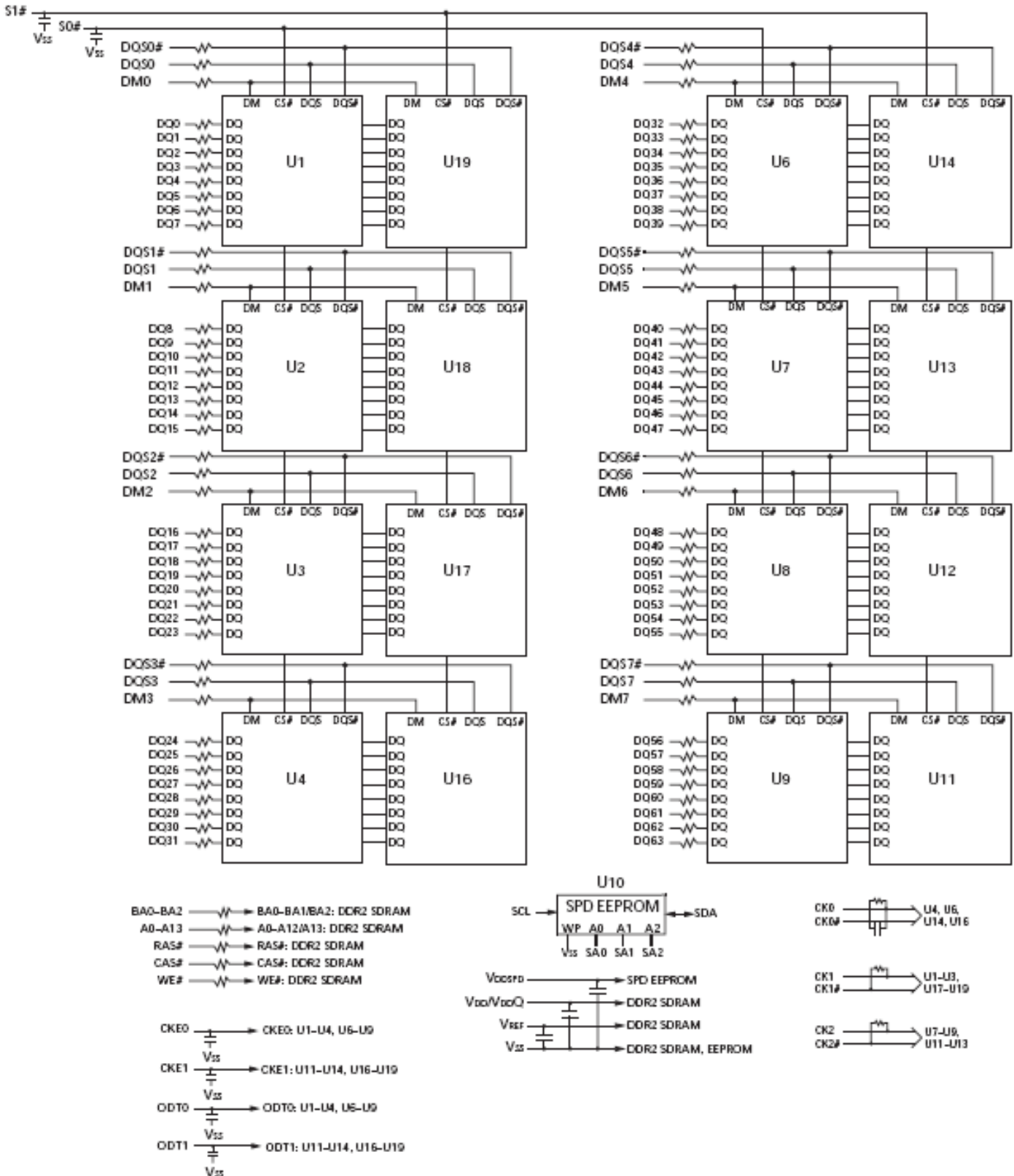
7.0 Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
128Mx8(1Gb) base	A0-A13	A0-A9	BA0-BA2	A10

240-Pin Unbuffered DIMM

DDR2 SDRAM

8.0 Functional Block Diagram: 2GB, 256Mx64 Module (Populated as 2 ranks of x8 SDRAM DDR2 Module)



9.0 AC & DC Operating Conditions

Recommended operating conditions (Voltage referenced to V_{SS}=0V, TA=0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V _{DD}	Supply Voltage	1.7	1.8	1.9	V
V _{DDL}	Supply Voltage for DLL	1.7	1.8	1.9	V
V _{DDO}	Supply Voltage for Output	1.7	1.8	1.9	V
V _{REF}	Input Reference Voltage	0.49*V _{DDQ}	0.50*V _{DDQ}	0.51*V _{DDQ}	mV
V _{TT}	Termination Voltage	V _{REF} -0.04	V _{REF}	V _{REF} +0.04	V

10.0 AC Timing Parameters & Specifications

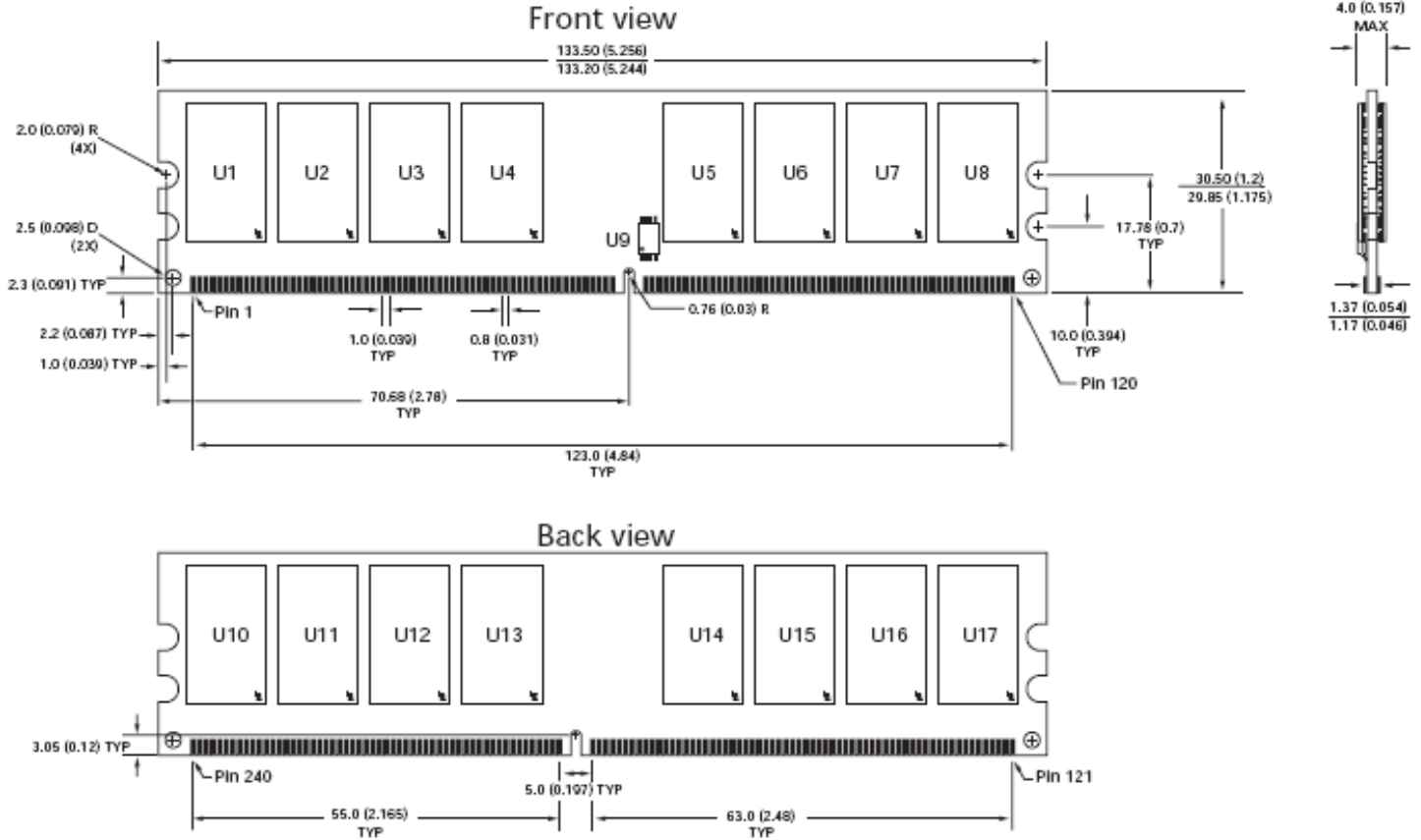
(AC operating conditions unless otherwise noted)

Parameter	Symbol	DDR2-800		Units
		min	max	
DQ output access time from $\overline{\text{CK}}/\text{CK}$	tAC	- 400	+400	ps
DQS output access time from $\overline{\text{CK}}/\text{CK}$	tDQSK	-350	+350	ps
CK high-level width	tCH	0.45	0.55	tCK
CK low-level width	tCL	0.45	0.55	tCK
CK half period	tHP	min(tCL,tCH)	x	ps
Clock cycle time, CL=x	tCK	2500	8000	ps
DQ and DM input hold time	tDH(base)	125	x	ps
DQ and DM input setup time	tDS(base)	50	x	ps
Control & Address input pulse width for each input	tIPW	0.6	x	tCK
DQ and DM input pulse width for each input	tDIPW	0.35	x	tCK
Data-out high-impedance time from $\overline{\text{CK}}/\text{CK}$	tHZ	x	tAC max	ps
DQS low-impedance time from $\overline{\text{CK}}/\text{CK}$	tLZ(DQS)	tAC min	tAC max	ps
DQ low-impedance time from $\overline{\text{CK}}/\text{CK}$	tLZ(DQ)	2*tAC min	tAC max	ps
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	200	ps
DQ hold skew factor	tQHS	x	300	ps
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	ps
First DQS latching transition to associated clock edge	tDQSS	-0.25	0.25	tCK
DQS input high pulse width	tDQSH	0.35	x	tCK
DQS input low pulse width	tDQSL	0.35	x	tCK
DQS falling edge to CK setup time	tDSS	0.2	x	tCK
DQS falling edge hold time from CK	tDSH	0.2	x	tCK
Mode register set command cycle time	tMRD	2	x	tCK

Parameter	Symbol	DDR2-800		Units
		min	max	
Write postamble	tWPST	0.4	0.6	tCK
Write preamble	tWPRE	0.35	x	tCK
Address and control input hold time	tIH(base)	250	x	ps
Address and control input setup time	tIS(base)	175	x	ps
Read preamble	tRPRE	0.9	1.1	tCK
Read postamble	tRPST	0.4	0.6	tCK
Active to active command period for 1KB page size products	tRRD	7.5	x	ns
Active to active command period for 2KB page size products	tRRD	10	x	ns
Four Activate Window for 1KB page size product	tFAW	35		ns
Four Activate Window for 2KB page size products	tFAW	45		ns
CAS to CAS command delay	tCCD	2	x	tCK
Write recovery time	tWR	15	x	ns
Auto pre-charge write recovery + pre-charge time	tDAL	WR+tRP	x	tCK
Internal write to read command delay	tWTR	7.5		ns
Internal read to pre-charge command delay	tRTP	7.5		ns
Exit self refresh to a non-read command	tXSNRt	tRFC + 10		ns
Exit self refresh to a read command	tXSRD	200		tCK
Exit pre-charge power down to any non-read command	tXP	2	x	tCK
Exit active power down to read command	tXARD	2	x	tCK
Exit active power down to read command (slow exit, lower power)	tXARDS	8 - AL		tCK
CKE minimum pulse width (high and low pulse width)	tCKE	3		tCK
ODT turn-on delay	tAOND	2	2	tCK
ODT turn-on	tAON	tAC(min)	tAC(max)+ 0.7	ns
ODT turn-on(Power-Down mode)	tAONPD	tAC(min)+2	2tCK+tAC(max)+1	ns
ODT turn-off delay	tAOFD	2.5	2.5	tCK
ODT turn-off	tAOF	tAC(min)	tAC(max)+ 0.6	ns
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5tCK+tAC(max)+1	ns
ODT to power down entry latency	tANPD	3		tCK
ODT power down exit latency	tAXPD	8		tCK
OCD drive mode output delay	tOIT	0	12	ns
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK +tIH		ns

**11.0 Physical Dimensions: (128Mx8 Based)
256Mx64 (2 Ranks)**

Units : Millimeters



Tolerances :± 0.005(.13) unless otherwise specified