DDR3 SODIMM Module

2GB based on 2Gbit component

TFBGA with Pb-Free

Revision 1.0 (JAN. 2008)
-Initial Release

1.0 Feature

- JEDEC standard 1.5V ± 0.075V Power Supply
- VDDQ = 1.5V ± 0.075V
- Programmable CAS Latency: 5,6,7,8,9,10,11,13
- Programmable Additive Latency(Posted CAS) : 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency(CWL) = 5 (DDR3-800), 6 (DDR3-1066), 7 (DDR3-1333), 8 (DDR3-1600) and 9 (DDR3-1866)
- Bi-directional Differential Data Strobe
- Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- On-Die termination using ODT pin
- 8 independent internal bank
- 400MHz fCK for 800Mb/sec/pin, 533MHz fCK for 1066Mb/sec/pin, 667MHz fCK for 1333Mb/sec/pin, 800MHz fCK for 1600Mb/sec/pin, 900MHz fCK for 1866Mb/sec/pin
- Asynchronous Reset
- Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Average Refresh Period 7.8us at lower than a TCASE 85°C, 3.9us at 85°C < TCASE < 95 °C
- Serial presence detect with EEPROM
- DIMM Dimension (Nominal) 30.00 mm high, 67.60 mm wide
- Based on JEDEC standard reference Raw Cards Lay out.
- RoHS compliant
- Gold plated contacts

2.0 Ordering Information

Part number	Density	Module Organization	Component composition	Component PKG	Module Rank	Description
W1333SA2Gx	2GB	256Mx64	256Mx8*8	TFBGA	1	2GB 1Rx8 PC3-10600U

Note: Last Character x of the Part Number stand for DRAM vendor
S=Samsung; M=Micron; H=Hynix

3.0 Key Timing Parameters

	DDR3-1333	Unit
CL-tRCD-tRP	9-9-9	tCK
CAS Latency	9	tCK
tCK(min)	1.5	ns
tRCD(min)	13.5	ns
tRP(min)	13.5	ns
tRAS(min)	36	ns
tRC(min)	49.5	ns

4.0 Absolute Maximum DC Rating

Symbol	Parameter	Rating	Units
V_{in} , Vout	Voltage on any pin relative to V_{SS}	-0.4 ~ 1.975	V
V_{DD}	Voltage on V_{DD} & V_{DDQ} supply relative to V_{ss}	-0.4 ~ 1.975	V
V_{DDQ}	Short circuit current	-0.4 ~ 1.975	V
V_{DDL}	Power dissipation	-0.4 ~ 1.975	V
T_{STG}	Storage Temperature	-55 ~ + 100	°C

5.0 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}DQ	2	Vss	71	Vss	72	Vss	139	Vss	140	DQ38
3	Vss	4	DQ4		KEY			141	DQ34	142	DQ39
5	DQ0	6	DQ5	73	CKE0	74	CKE1	143	DQ35	144	Vss
7	DQ1	8	Vss	75	V_{DD}	76	V_{DD}	145	Vss	146	DQ44
9	Vss	10	*/DQS0*	77	NC	78	A15	147	DQ40	148	DQ45
11	*DM0*	12	*DQS0*	79	BA2	80	A14	149	DQ41	150	Vss
13	Vss	14	Vss	81	V_{DD}	82	V_{DD}	151	Vss	152	*/DQS5*
15	DQ2	16	DQ6	83	A12/$\overline{BC}$	84	A11	153	*DM5*	154	*DQS5*
17	DQ3	18	DQ7	85	A9	86	A7	155	Vss	156	Vss
19	Vss	20	Vss	87	V_{DD}	88	V_{DD}	157	DQ42	158	DQ46
21	DQ8	22	DQ12	89	A8	90	A6	159	DQ43	160	DQ47
23	DQ9	24	DQ13	91	A5	92	A4	161	Vss	162	Vss
25	Vss	26	Vss	93	V_{DD}	94	V_{DD}	163	DQ48	164	DQ52
27	*/DQS1*	28	*DM1*	95	A3	96	A2	165	DQ49	166	DQ53
29	*DQS1*	30	*/RESET*	97	A1	98	A0	167	V_{SS}	168	Vss
31	Vss	32	Vss	99	V_{DD}	100	V_{DD}	169	*/DQS6*	170	*DM6*
33	DQ10	34	DQ14	101	*/CK0*	102	*CK1*	171	*DQS6*	172	Vss
35	DQ11	36	DQ15	103	*CK0*	104	*/CK1*	173	Vss	174	DQ54
37	Vss	38	Vss	105	V_{DD}	106	V_{DD}	175	DQ50	176	DQ55
39	DQ16	40	DQ20	107	A10/AP	108	BA1	177	DQ51	178	Vss
41	DQ17	42	DQ21	109	BA0	110	/RAS	179	Vss	180	DQ60
43	Vss	44	Vss	111	V_{DD}	112	V_{DD}	181	DQ56	182	DQ61
45	*/DQS2*	46	*DM2*	113	/WE	114	/S0	183	DQ57	184	Vss
47	*DQS2*	48	Vss	115	/CAS	116	ODT0	185	Vss	186	*/DQS7*
49	Vss	50	DQ22	117	V_{DD}	118	V_{DD}	187	*DM7*	188	*DQS7*
51	DQ18	52	DQ23	119	A13	120	ODT1	189	Vss	190	Vss
53	DQ19	54	Vss	121	/S1	122	NC	191	DQ58	192	DQ62
55	Vss	56	DQ28	123	V_{DD}	124	V_{DD}	193	DQ59	194	DQ63
57	DQ24	58	DQ29	125	TEST	126	V_{REF}CA	195	Vss	196	Vss
59	DQ25	60	Vss	127	Vss	128	Vss	197	SA0	198	*NC*
61	Vss	62	*/DQS3*	129	DQ32	130	DQ36	199	V_{DD}SPD	200	SDA
63	DM3	64	*DQS3*	131	DQ33	132	DQ37	201	SA1	202	SCL
65	Vss	66	Vss	133	Vss	134	Vss	203	Vtt	204	Vtt
67	DQ26	68	DQ30	135	*/DQS4*	136	*DM4*				
69	DQ27	70	DQ31	137	*DQS4*	138	Vss				

NC = No Connect, RFU = Reserved for Future Use

6.0 DIMM Pin Description

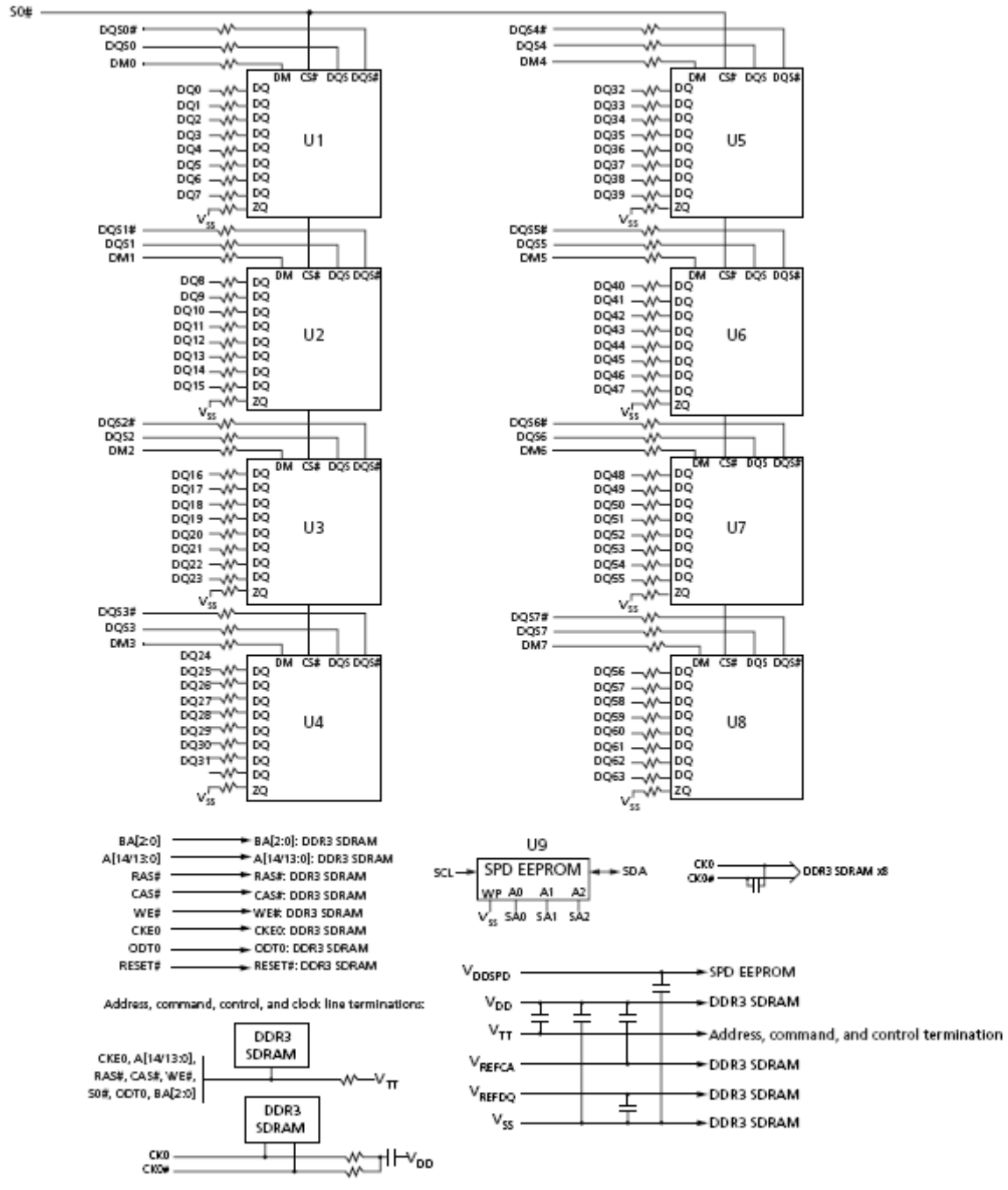
Pin Name	Function	Pin Name	Function
A0 ~ A15	Address input (Multiplexed)	ODT0~ODT1	On Die Termination
A10/AP	Address Input/Auto pre-charge	CB0~CB7	ECC Data check bits Input/Output
BA0 ~ BA2	Bank Select	DQ0~DQ63	Data Input/Output
/CK0 ~ /CK2, CK0~CK2	Clock input	/DQS0~/DQS8	Data strobes, negative line
CKE0, CKE1	Clock enable input	DM(0~8),	Data Masks/Data strobes (Read)
/S0, /S1	Chip select input	DQS0~DQS8	Data Strobes
/RAS	Row address strobe	RFU	Reserved for future used
/CAS	Column address strobe	V_{TT}	SDRAM I/O termination power supply
/WE	Write Enable	TEST	Memory bus test tool
SCL	SPD Clock Input	V_{DD}	Core Power
SDA	SPD Data Input/Output	V_{DDQ}	I/O Power
SA0~SA2	SPD Address	V_{SS}	Ground
Par_In	Parity bit for address & Control bus	V_{REF}DQ	SDRAM Input/Output Reference Supply
Err_Out	Parity error found in the Address and Control bus	V_{DD}SPD	Serial EEPROM Power Supply
/RESET	Register and PLL control pin	V_{REF}CA	Command Address Reference Supply

7.0 Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Pre-charge
256Mx8(2Gb) base	A0-A14	A0-A9	BA0-BA2	A10/AP

8.0 Functional Block Diagram:

2GB, 256Mx64 Module Populated as 1 rank of x8)



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

9.0 AC & DC Operating Conditions

Recommended operating conditions (Voltage referenced to Vss=0V, TA=0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	1.425	1.5	1.575	V
V_{DDQ}	Supply Voltage for Output	1.425	1.5	1.575	V
$V_{REF}DQ_{(DC)}$	I/O Reference Voltage (DQ)	$0.49*V_{DDQ}$	$0.50*V_{DDQ}$	$0.51*V_{DDQ}$	V
$V_{REF}CA_{(DC)}$	I/O Reference Voltage (CMD/Add)	$0.49*V_{DDQ}$	$0.50*V_{DDQ}$	$0.51*V_{DDQ}$	V
V_{TT}	Termination Voltage	$0.49*V_{DDQ}$	$0.50*V_{DDQ}$	$0.51*V_{DDQ}$	V

10.0Capacitance (Max.)

Symbol	Parameter/Condition	Min	Max	Unit
CCK	Input capacitance, CK and $\overline{CK}$	-	11	pF
CI1	Input capacitance, CKE and $\overline{CS}$	-	12	pF
CI2	Input capacitance, Addr, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	-	12	pF
CIO	Input capacitance, DQ, DM, DQS, $\overline{DQS}$	-	10	pF

11.1 AC Timing Parameters & Specifications

(AC operating conditions unless otherwise noted)

Parameter	Symbol	DDR3-1333		Units
		min	max	
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	ns
Average Clock Period	tCK(avg)	-		ps
Clock Period	tCK(abs)	tCK(avg) min +tJIT (per)min	tCK(avg) max +tJIT (per)max	ps
Average high pulse width	tCH(avg)	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	tCK(avg)
Clock Period Jitter	tJIT(per)	-80	80	ps
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-80	80	ps
Cycle to Cycle Period Jitter	tJIT(cc)	160	-	ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	140	-	ps
Cumulative error across 2 cycles	tERR(2per)	- 118	118	ps
Cumulative error across 3 cycles	tERR(3per)	- 140	140	ps
Cumulative error across 4 cycles	tERR(4per)	- 155	155	ps
Cumulative error across 5 cycles	tERR(5per)	- 168	168	ps
Cumulative error across 6 cycles	tERR(6per)	- 177	177	ps
Cumulative error across 7 cycles	tERR(7per)	- 186	186	ps
Cumulative error across 8 cycles	tERR(8per)	- 193	193	ps
Cumulative error across 9 cycles	tERR(9per)	- 200	200	ps
Cumulative error across 10 cycles	tERR(10per)	- 205	205	ps

11.2 AC Timing Parameters & Specifications (con't)

Parameter	Symbol	DDR3-1333		Units
		min	max	
Cumulative error across 11 cycles	tERR(11per)	- 210	210	ps
Cumulative error across 12 cycles	tERR(12per)	- 215	215	ps
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 = 0.68ln(n))*tJIT(per)max		ps
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	tCK(avg)
Absolute clock Low pulse width	tCL(abs)	0.43	-	tCK(avg)
Data Timing				
DQS, /DQS to DQ skew, per group, per access	tDQSQ	-	125	ps
DQ output hold time from DQS, /DQS	tQH	0.38	-	tCK(avg)
DQ low-impedance time from CK, /CK	tLZ(DQ)	-500	250	ps
DQ high-impedance time from CK, /CK	tHZ(DQ)	-	250	ps
Data setup time to DQS, /DQS referenced to Vih(ac)Vil(ac) levels	tDS(base)	TBD	-	ps
Data hold time to DQS, /DQS referenced to Vih(ac)Vil(ac) levels	tDH(base)	TBD	-	ps
DQ and DM Input pulse width for each input	tDIPW	400	-	ps
Data Strobe Timing				
DQS, /DQS READ Preamble	tRPRE	0.9	-	tCK
DQS, /DQS differential READ Postamble	tRPST	0.3	-	tCK
DQS, /DQS output high time	tQSH	0.4	-	tCK(avg)
DQS, /DQS output low time	tQSL	0.4	-	tCK(avg)
DQS, /DQS WRITE Preamble	tWPRE	0.9	-	tCK
DQS, /DQS WRITE Postamble	tWPST	0.3	-	tCK
DQS, /DQS rising edge output access time from rising CK, /CK	tDQSCK	-255	255	ps
DQS, /DQS low-impedance time (Referenced from RL-1)	tLZ(DQS)	-500	250	ps
DQS, /DQS high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	250	-	ps
DQS, DQS differential input low pulse width	tDQSL	0.45	0.55	tCK
DQS, DQS differential input high pulse width	tDQSH	0.45	0.55	tCK
DQS, DQS rising edge to CK, CK rising edge	tDQSS	-0.25	0.25	tCK(avg)
DQS,DQS faling edge setup time to CK, CK rising edge	tDSS	0.2	-	tCK(avg)
DQS,DQS faling edge hold time to CK, CK rising edge	tDSH	0.2	-	tCK(avg)
DLL locking time	tDLLK	512	-	nCK
internal READ Command to PRECHARGE Command delay	tRTP	max (4tCK,7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max (4tCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	nCK
Mode Register Set command update delay	tMOD	max (12tCK,15ns)	-	
CAS# to CAS# command delay	tCCD	4	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(AVG))		nCK

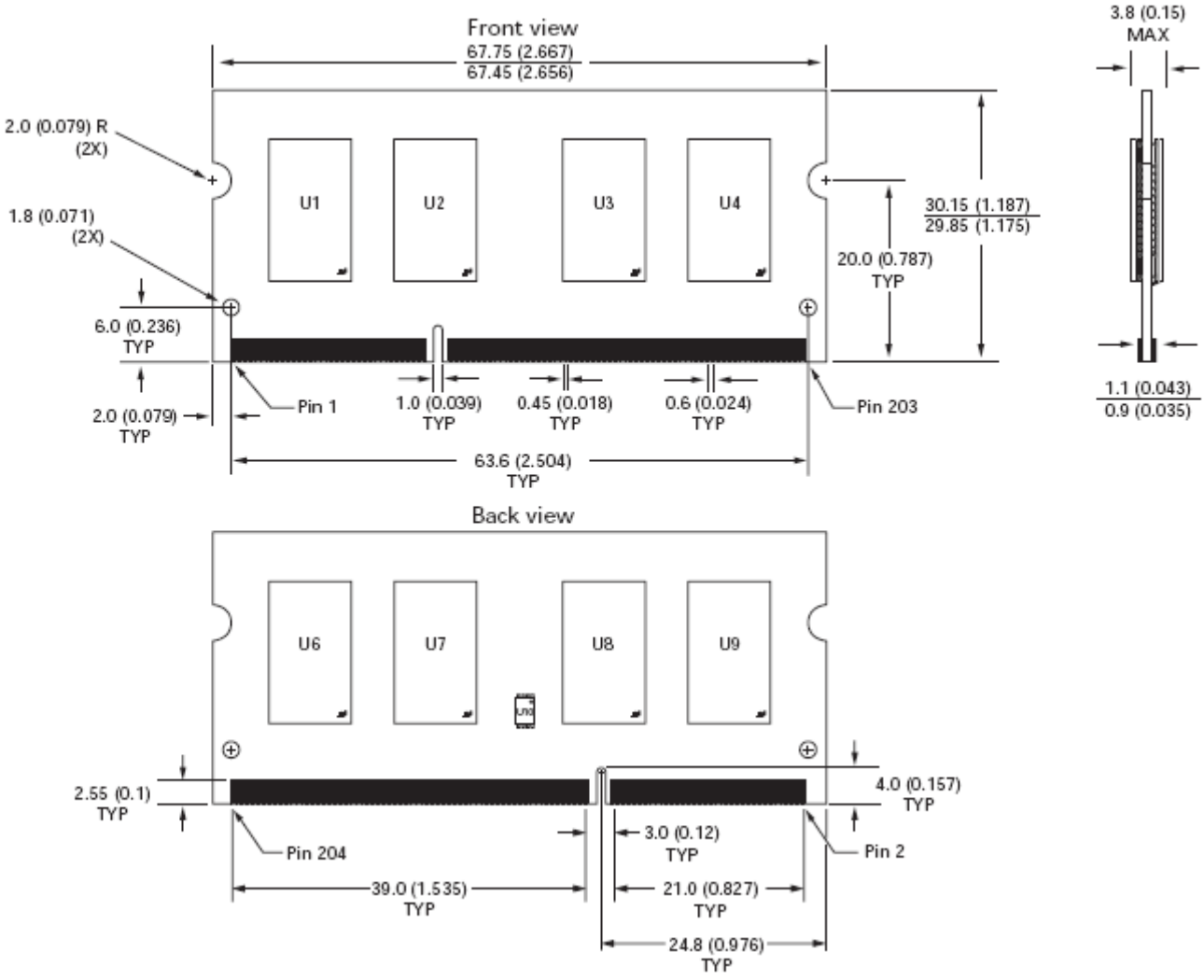
11.3 AC Timing Parameters & Specifications (con't)

Parameter	Symbol	DDR3-1333		Units
		min	max	
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK
ACTIVE to PRECHARGE command period	tRAS	36	70,000	ns
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max(4tCK,6ns)	-	
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max(4tCK,7.5ns)	-	
Four activate window for 1KB page size	tFAW	30	-	ns
Four activate window for 2KB page size	tFAW	45	-	ns
Command and Address setup time to CK, CK referenced to Vih(ac) / Vil(ac) levels	tIS(base)	65	-	ps
Command and Address hold time from CK, CK referenced to Vih(ac) / Vil(ac) levels	tIH(base)	140	-	ps
Command and Address setup time to CK, CK referenced to Vih(ac) / Vil(ac) levels	tIS(base)AC150	65+125	-	ps
Control & Address Input pulse width for each input	tIPW	620	-	ps
Calibration Timing				
Power-up and RESET calibration time	tZQinitI	512	-	tCK
Normal operation Full calibration time	tZQoper	256	-	tCK
Normal operation short calibration time	tZQCS	64	-	tCK
Reset Timing				
Exit Reset from CKE HIGH to a valid command	tXPR	max(5tCK, tRFC+10ns)	-	
Self Refresh Timing				
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5tCK,tRFC+ 10ns)	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	nCK
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE)	tCKSRE	max(5tCK, 10ns)	-	
Valid Clock Requirement before Self Refresh Exit (SRX)	tCKSRX	max(5tCK, 10ns)	-	
Power Down Timing				
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLLfrozen to commands not requiring a locked DLL	tXP	max(3tCK,6ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max(10tCK, 24ns)	-	
CKE minimum pulse width	tCKE	max(3tCK, 5.625ns)	-	
Command pass disable delay	tCPDED	1	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCK
Timing of ACT command to Power Down entry	tACTPDEN	1	-	nCK
Timing of PRE command to Power Down entry	tPRPDEN	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 +1	-	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRPDEN	WL + 4 +(tWR/tCK)	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN	WL + 4 +WR+1	-	nCK
Timing of WR command to Power Down entry (BL4MRS)	tWRPDEN	WL + 2 +(tWR/ tCK(avg))	-	nCK

11.4 AC Timing Parameters & Specifications (con't)

Parameter	Symbol	DDR3-1333		Units
		min	max	
Timing of WRA command to Power Down entry (BL4MRS)	tWRAPDEN	WL +2 +WR +1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	1	-	
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	
ODT Timing				
ODT high time without write command or with wirte commandand BC4	ODTH4	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	nCK
Asynchronous RTT tum-on delay (Power-Down with DLL frozen)	tAONPD	1	9	ns
Asynchronous RTT tum-off delay (Power-Down with DLL frozen)	tAOFPD	1	9	ns
ODT turn-on	tAON	-250	250	ps
RTT_NOM and RTT_WR turn-off time from ODTL off reference	tAOF	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)
Write Leveling Timing				
First DQS pulse rising edge after tDQSS margining mode is programmed	tWLMRD	40	-	tCK
DQS/DQS delay after tDQS margining mode is programmed	tWLDQSEN	25	-	tCK
Setup time for tDQSS latch	tWLS	195	-	ps
Hold time of tDQSS latch	tWLH	195	-	ps
Write leveling output delay	tWLO	0	9	ns
Write leveling output error	tWLOE	0	2	ns

12.0 Physical Dimensions: (256Mbx8 Based, 256MBx64, 1 Rank)



Units: Millimeter
Tolerances: ± 0.13) unless otherwise specified