

DDR3L-1.35V
Load Reduced DIMM Module

32GB based on 8Gbit-DDP component

FBGA with Pb-Free



Revision 1.0 (Oct. 2013)
-Initial Release

1.0 Feature

- JEDEC standard Double Data Rate3L Synchronous DRAMs(DDR3L SDRAMs) with 1.35V nominal
- Buffer performance by LRDIMM presenting less load to sytem
- Compatible with RDIMM systems with appropriate BIOS changes
- Backward Compatible with 1.5V DDR3 Memory Module
- Data transfer rates: PC3-10600, PC3-8500
- Functionality and operations comply with the DDR3L SDRAM datasheet
- Host interface and MB(Memory Buffer) component industry standard compliant
- MB provides “address multiplication” to generate additional chips selects
- Address mirroring
- ODT (On-Die Termination)
- Built with 2Gb DDR3 SDRAMs in 82ball FBGA
- 240 pin Load Reduced DDR3 DRAM Dual-Line Memory Module
- 133.35 x 30.35 mm form factor
- Full DIMM Heat Spreader
- Serial presence detect with EEPROM
- Based on JEDEC standard reference Raw Cards Lay out.
- RoHS compliant
- Gold plated contacts

2.0 Ordering Information

Part number	Density	Module Organization	Component composition	Component PKG	Module Rank	Description
W16LQ32GLS	32GB	4Gx72	2Gx4-DDP*36	FBGA	4	PC3-12800

Note: Last Character of the Part Number stand for DRAM vendor
S=Samsung; M=Micron; H=Hynix

3.0 Operating Frequencies

	DDR3-1600	Unit
CL-tRCD-tRP	11-11-11	tCK
CAS Latency	11	tCK
tCK(min)	1.25	ns
tRCD(min)	13.5	ns
tRP(min)	13.5	ns
tRAS(min)	35	ns
tRC(min)	48.75	ns

4.0 Absolute Maximum DC Rating

Symbol	Parameter	Rating	Units
V_{in}, V_{out}	Voltage on any pin relative to V_{SS}	-0.4 ~ 1.975	V
V_{DD}	Voltage on V_{DD} & V_{DDQ} supply relative to V_{SS}	-0.4 ~ 1.975	V
V_{DDQ}	Short circuit current	-0.4 ~ 1.975	V
V_{DDL}	Power dissipation	-0.4 ~ 1.975	V
T_{STG}	Storage Temperature	-55 ~ + 100	°C

5.0 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V _{REF} DQ	121	V _{SS}	31	DQ25	151	V _{SS}
2	V _{SS}	122	DQ4	32	V _{SS}	152	DM3,DQS12, TDQS12
3	DQ0	123	DQ5	33	$\overline{\text{DQS}}3$	153	NC, DQS12, TDQS12
4	DQ1	124	V _{SS}	34	DQS3	154	V _{SS}
5	V _{SS}	125	DM0,DQS9, TDQS9	35	V _{SS}	155	DQ30
6	$\overline{\text{DQS}}0$	126	NC, $\overline{\text{DQS}}9$, TDQS9	36	DQ26	156	DQ31
7	DQS0	127	V _{SS}	37	DQ27	157	V _{SS}
8	V _{SS}	128	DQ6	38	V _{SS}	158	CB4,NC
9	DQ2	129	DQ7	39	CB0,NC	159	CB5,NC
10	DQ3	130	V _{SS}	40	CB1,NC	160	V _{SS}
11	V _{SS}	131	DQ12	41	V _{SS}	161	NC,DQM8,DQS17, TDQS17
12	DQ8	132	DQ13	42	$\overline{\text{DQS}}8$	162	NC, $\overline{\text{DQS}}17$ TDQS17
13	DQ9	133	V _{SS}	43	DQS8	163	V _{SS}
14	V _{SS}	134	DM0,DQS10, TDQS0	44	V _{SS}	164	CB6,NC
15	$\overline{\text{DQS}}1$	135	NC, $\overline{\text{DQS}}10$ TDQS10	45	CB2,NC	165	CB7,NC
16	DQS1	136	V _{SS}	46	CB3,NC	166	V _{SS}
17	V _{SS}	137	DQ14	47	V _{SS}	167	NC
18	DQ10	138	DQ15	48	V _{TT} , NC	168	RESET
19	DQ11	139	V _{SS}	KEY			
20	V _{SS}	140	DQ20	49	V _{TT} ,NC	169	CKE1,NC
21	DQ16	141	DQ21	50	CKE0	170	V _{DD}
22	DQ17	142	V _{SS}	51	V _{DD}	171	A15
23	V _{SS}	143	DM2,DQS11, TDQS11	52	BA2	172	A14
24	$\overline{\text{DQS}}2$	144	NC, DQS11, TDQS11	53	$\overline{\text{ERR_OUT}}$,NC	173	V _{DD}
25	DQS2	145	V _{SS}	54	V _{DD}	174	A12/BC
26	V _{SS}	146	DQ22	55	A11	175	A9
27	DQ18	147	DQ23	56	A7	176	V _{DD}
28	DQ19	148	V _{SS}	57	V _{DD}	177	A8
29	V _{SS}	149	DQ28	58	A5	178	A6
30	DQ24	150	DQ29	59	A4	179	V _{DD}
				60	V _{DD}	180	A3

5.1 DIMM Configurations Cont' (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back
61	A2	181	A1	91	DQ41	211	V _{SS}
62	V _{DD}	182	V _{DD}	92	V _{SS}	212	DM5,DQS14, TDQS14
63	NC,Ck1	183	V _{DD}	93	$\overline{\text{DQS5}}$	213	$\overline{\text{NC,DQS14}},$ $\overline{\text{TDQS14}}$
64	NC, $\overline{\text{Ck1}}$	184	CK0	94	DQS5	214	V _{SS}
65	V _{DD}	185	$\overline{\text{CK0}}$	95	V _{SS}	215	DQ46
66	V _{DD}	186	V _{DD}	96	DQ42	216	DQ47
67	V _{REF} CA	187	$\overline{\text{EVENT}}$	97	DQ43	217	V _{SS}
68	NC/Par_in	188	A0	98	V _{SS}	218	DQ52
69	V _{DD}	189	V _{DD}	99	DQ48	219	DQ53
70	A10/AP	190	BA1	100	DQ49	220	V _{SS}
71	BA0	191	V _{DD}	101	V _{SS}	221	DM6,DQS15, TDQS15
72	V _{DD}	192	$\overline{\text{RAS}}$	102	$\overline{\text{DQS6}}$	222	$\overline{\text{NC,DQS15}},$ $\overline{\text{TDQS15}}$
73	$\overline{\text{WE}}$	193	$\overline{\text{S0}}$	103	DQS6	223	V _{SS}
74	$\overline{\text{CAS}}$	194	V _{DD}	104	V _{SS}	224	DQ54
75	V _{DD}	195	ODT0	105	DQ50	225	DQ55
76	NC, $\overline{\text{S1}}$	196	A13	106	DQ51	226	V _{SS}
77	NC,ODT1	197	V _{DD}	107	V _{SS}	227	DQ60
78	V _{DD}	198	NC, $\overline{\text{S3}}$	108	DQ56	228	DQ61
79	NC, $\overline{\text{S2}}$	199	V _{SS}	109	DQ57	229	V _{SS}
80	V _{SS}	200	DQ36	110	V _{SS}	230	DM7,DQS16, TDQS16
81	DQ32	201	DQ37	111	$\overline{\text{DQS7}}$	231	$\overline{\text{NC,DQS16}},$ $\overline{\text{TDQS16}}$
82	DQ33	202	V _{SS}	112	DQS7	232	V _{SS}
83	V _{SS}	203	DM4,DQS13, TDQS13	113	V _{SS}	233	DQ62
84	$\overline{\text{DQS4}}$	204	$\overline{\text{NC,DQS13}},$ $\overline{\text{TDQS13}}$	114	DQ58	234	DQ63
85	DQS4	205	V _{SS}	115	DQ59	235	V _{SS}
86	V _{SS}	206	DQ38	116	V _{SS}	236	V _{DD} SPD
87	DQ34	207	DQ39	117	SA0	237	SA1
88	DQ35	208	V _{SS}	118	SCL	238	SDA
89	V _{SS}	209	DQ44	119	SA2	239	V _{SS}
90	DQ40	210	DQ45	120	V _{TT}	240	V _{TT}

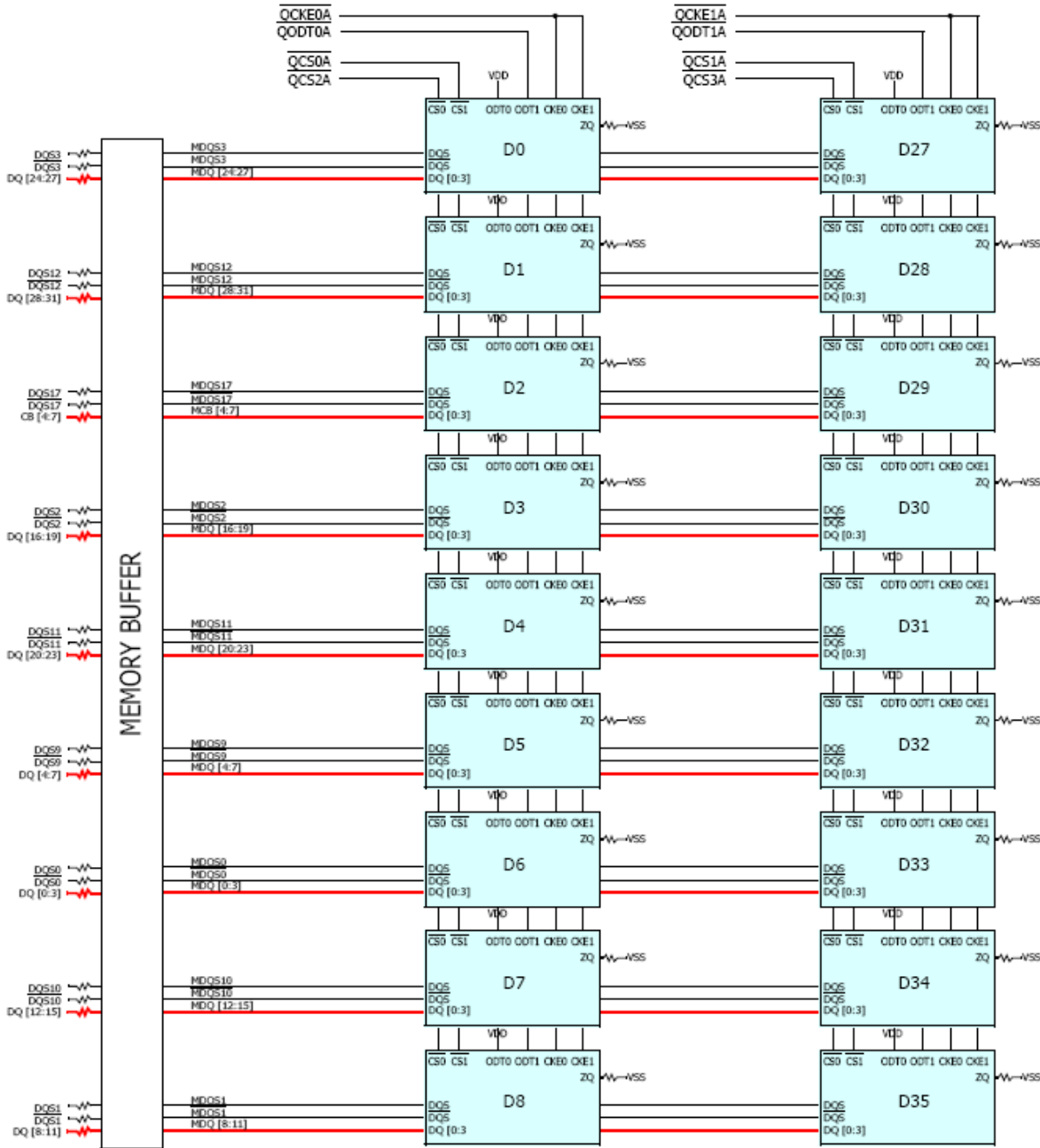
6.0 DIMM Pin Description

Pin Name	Function	Pin Name	Function
A0 ~ A15	Address input (Multiplexed)	ODT0~ODT1	On Die Termination
A10/AP	Address Input/Auto pre-charge	$\overline{\text{Err_Out}}$	Parity error found on the Address and Control bus
$\overline{\text{A12/BC}}$	Address Input/Burst chop	CB0~CB7	ECC Data check bits Input/Output
BA0 ~ BA2	Bank Select	DQ0~DQ63	Data Input/Output
$\overline{\text{CK0}} \sim \overline{\text{CK3}}$, CK0 ~ CK3	Clock input Clock input, negative line	$\overline{\text{DQS0}} \sim \overline{\text{DQS8}}$	Data strobes, negative line
CKE0, CKE1	Clock enable input	DQS0~DQS8	Data Strobes
$\overline{\text{S0}} \sim \overline{\text{S3}}$	Chip select input	DM (0~8),	Data Masks/Data strobes (Read)
$\overline{\text{RAS}}$	Row address strobe	DQS9~DQS17 TDQS9~TDQS17	Data Strobes Termination data strobes
$\overline{\text{CAS}}$	Column address strobe	$\overline{\text{DQS9}} \sim \overline{\text{DQS17}}$ TDQS9~TDQS17	Data Strobes, negative line Termination data strobes, negative line
$\overline{\text{WE}}$	Write Enable	V _{TT}	SDRAM I/O termination power supply
SCL	SPD Clock Input	TEST	Memory bus test tool
SDA	SPD Data Input/Output	V _{DD}	Core Power
SA0~SA2	SPD Address	V _{SS}	Ground
Par_In	Parity bit for address & Control bus	V _{REFDQ}	SDRAM Input/Output Reference Supply
$\overline{\text{EVENT}}$	EVENT pin on TS/SPD part, Temperature event	V _{DDSPD}	Serial EEPROM Power Supply
$\overline{\text{RESET}}$	Register and PLL control pin	V _{REFCA}	Command Address Reference Supply

7.0 Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Pre-charge
2Gx4(8Gb DDP) based	A0-A15	A0-A9, A11,A13	BA0-BA2	A10/AP

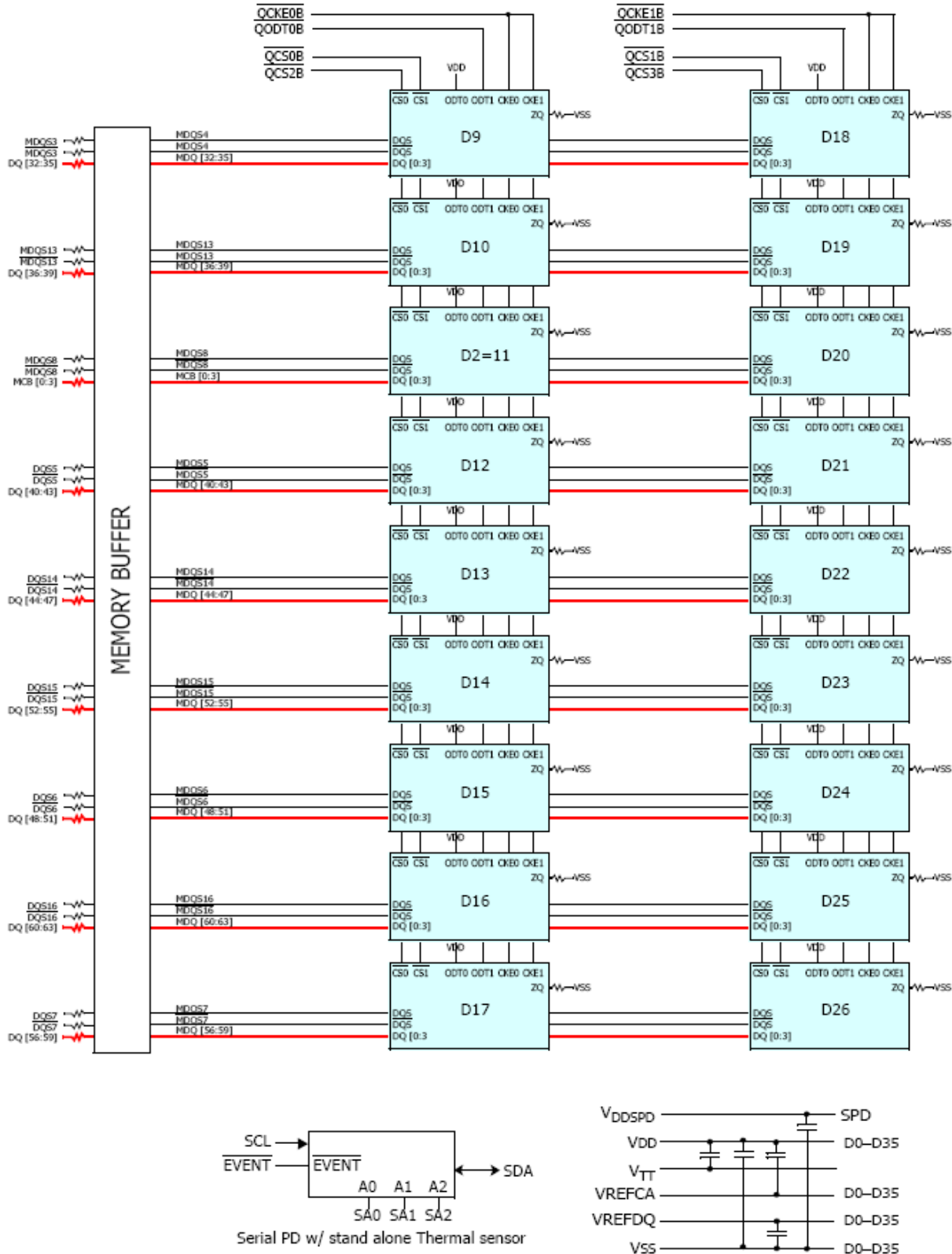
8.0 Functional Block Diagram: 32GB/2Gx72 Module (Populated as 4 ranks of x4 SDRAM Module)



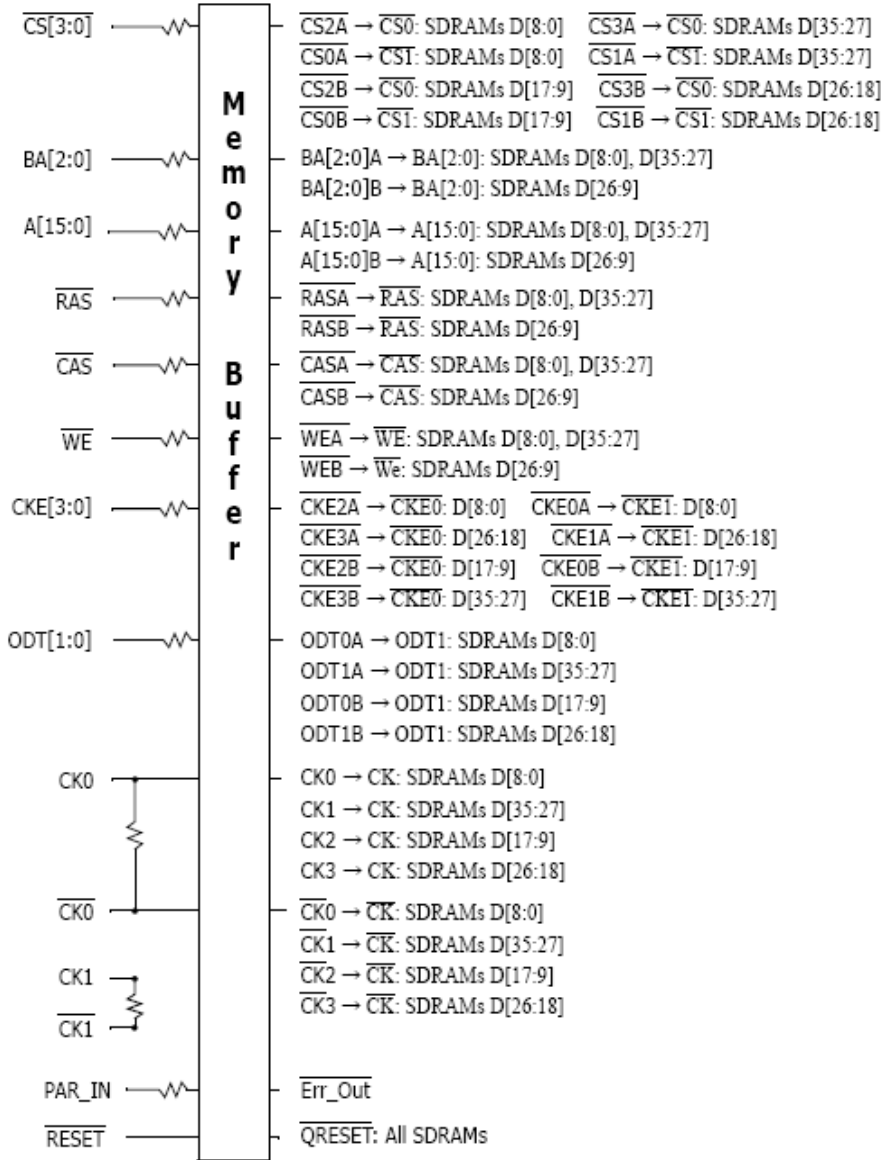
Notes:

1. Unless otherwise noted, resistor values are 10 Ohms ±5%.
2. See the wiring diagrams for all resistors associated with the command, address and control bus.
3. This Design uses SDRAMz in DDR. There are four ZQ resistors per DDR. The ZQ resistors are 240 Ohms ±1%.
4. DM pins on SDRAMs are wired to VSS.
5. The DQ and MDQ labels reflect the byte lanes as defined at the edge connector not which Memory Buffer pins are used.

8.1 Functional Block Diagram: 32GB/4Gx72 Module (Populated as 4 ranks of x4 SDRAM Module)



8.2 Functional Block Diagram: 32GB/4Gx72 Module (Populated as 4 ranks of x4 SDRAM Module)



1. CK0 and $\overline{CK0}$ are terminated with 120 Ohms $\pm 5\%$ resistor.
2. CK1 and $\overline{CK1}$ are terminated with 120 Ohms $\pm 5\%$ resistor, but is not used.
3. Unless otherwise noted resistors are 22 Ohms $\pm 5\%$

9.0 AC & DC Operating Conditions

Recommended operating conditions DDR3L (1.35V) operation

Symbol	Parameter	Min	Typ	Max	Unit
V _{DD}	Supply Voltage	1.283	1.35	1.45	V
V _{DDQ}	Supply Voltage for Output	1.283	1.35	1.45	V

Recommended operating conditions DDR3L (1.5V) operation

Symbol	Parameter	Min	Typ	Max	Unit
V _{DD}	Supply Voltage	1.425	1.5	1.575	V
V _{DDQ}	Supply Voltage for Output	1.425	1.5	1.575	V

10.0 DRAM Component Operating Temperature Range

Symbol	Parameter/Condition	Rating	Unit
T _{OPER}	Normal Operating Temperature Range	0 to 85	°C
	Extended Temperature Range	85 to 95	°C

11.1 AC Timing Parameters & Specifications

(AC operating conditions unless otherwise noted)

Parameter	Symbol	DDR3-800		Units	Note	
		min	max			
Internal read command to first data	tAA	15	20	ns		
ACT to internal read or write delay time	tRCD	15	-	ns		
PRE command period	tRP	15	-	ns		
ACT to ACT or REF command period	tRC	52.5	-	ns		
ACT to PRE command period	tRAS	37.5	9 * tREFI	ns		
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3
Supported CL Settings		6		nCK		
Supported CWL Settings		5		nCK		

11.2 AC Timing Parameters & Specifications(con't)

Parameter	Symbol	DDR3-1066		Units	Note	
		min	max			
Internal read command to first data	tAA	13.125	20	ns		
ACT to internal read or write delay time	tRCD	13.125	-	ns		
PRE command period	tRP	13.125	-	ns		
ACT to ACT or REF command period	tRC	50.625	-	ns		
ACT to PRE command period	tRAS	37.5	9 * tREFI	ns		
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,6
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	< 2.5	ns	1,2,3,4
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	< 2.5	ns	1,2,3
Supported CL Settings		6, 7, 8		nCK		
Supported CWL Settings		5, 6		nCK		

11.3 AC Timing Parameters & Specifications(con't)

Parameter		Symbol	DDR3-1333		Units	Note
			min	max		
Internal read command to first data		tAA	13.5	20	ns	
ACT to internal read or write delay time		tRCD	13.5	-	ns	
PRE command period		tRP	13.5	-	ns	
ACT to ACT or REF command period		tRC	49.5	-	ns	
ACT to PRE command period		tRAS	36	9 * tREFI	ns	
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,7
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4,7
	CWL = 7	tCK(AVG)	Reserved		ns	4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	< 2.5	ns	1,2,3,4,7
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	< 2.5	ns	1,2,3,4,7
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,4
CL = 10	CWL = 5, 6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3
		tCK(AVG)	Reserved		ns	5
Supported CL Settings			6, 8, 7, 9, 10		nCK	
Supported CWL Settings			5, 6, 7		nCK	

11.4 AC Timing Parameters & Specifications(con't)

Parameter		Symbol	DDR3-1600		Units	Note
			min	max		
Internal read command to first data		tAA	13.75	20	ns	
ACT to internal read or write delay time		tRCD	13.75	-	ns	
PRE command period		tRP	13.75	-	ns	
ACT to ACT or REF command period		tRC	48.75	-	ns	
ACT to PRE command period		tRAS	35	9 * tREFI	ns	
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,8
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CWL = 7	tCK(AVG)	Reserved			4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	< 2.5	ns	1,2,3,4,8
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CWL = 8	tCK(AVG)	Reserved		ns	4
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	< 2.5	ns	1,2,3,8
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	< 1.875	ns	1,2,3,4,8
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 10	CWL = 5, 6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	< 1.875	ns	1,2,3,8
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 11	CWL = 5, 6, 7	tCK(AVG)	Reserved		ns	4
	CWL = 8	tCK(AVG)	1.25	< 1.5	ns	1,2,3
Supported CL Settings			5, 6, 7, 8, 9, 10, 11		nCK	
Supported CWL Settings			5, 6, 7, 8		nCK	

11.5 AC Timing Parameters & Specifications(con't)

Parameter		Symbol	DDR3-1866		Units	Note
			min	max		
Internal read command to first data		tAA	13.91	20	ns	
ACT to internal read or write delay time		tRCD	13.91	-	ns	
PRE command period		tRP	13.91	-	ns	
ACT to ACT or REF command period		tRC	47.91	-	ns	
ACT to PRE command period		tRAS	34	9 * tREFI	ns	
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,9
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CWL = 7, 8, 9	tCK(AVG)	Reserved			4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	< 2.5	ns	1,2,3,4,9
	CWL = 7, 8, 9	tCK(AVG)	Reserved		ns	4
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	< 2.5	ns	1,2,3,9
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CWL = 8, 9	tCK(AVG)	Reserved		ns	4
CL = 9	CWL = 5, 6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,4,9
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CWL = 9	tCK(AVG)	Reserved		ns	4
CL = 10	CWL = 5, 6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,9
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4,9
CL = 11	CWL = 5, 6, 7	tCK(AVG)	Reserved		ns	4
	CWL = 8	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,9
	CWL = 9	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 12	CWL = 5, 6, 7, 8	tCK(AVG)	Reserved		ns	4
	CWL = 9	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 13	CWL = 5, 6, 7, 8	tCK(AVG)	Reserved		ns	4
	CWL = 9	tCK(AVG)	1.07	<1.25	ns	1,2,3
Supported CL Settings			5, 6, 7, 8, 9, 10, 11, 13		nCK	
Supported CWL Settings			5, 6, 7, 8, 9		nCK	

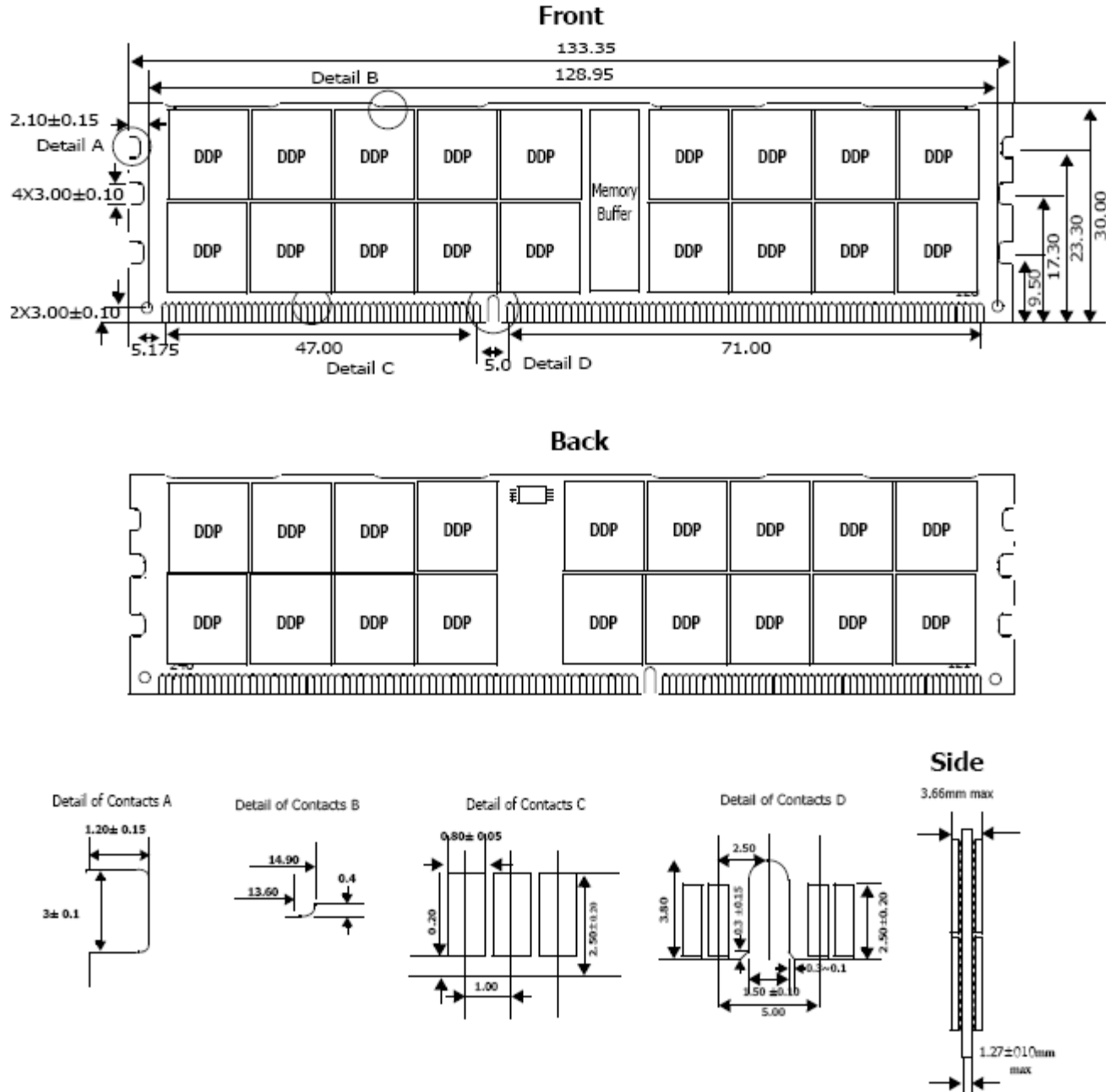
Speed Bin Table Notes

Absolute Specification (TOPER; VDDQ = VDD = 1.35V +1.000/- 0.067 V);

(TOPER; VDDQ = VDD = 1.5V +/- 0.075 V);

- 1.The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
- 2.tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (3.0, 2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL', where tCK(AVG) = 3.0 ns should only be used for CL = 5 calculation.
- 3.tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
- 4.'Reserved' settings are not allowed. User must program a different value.
- 5.'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to DIMM data sheet and/or the DIMM SPD information if and how this setting is supported.
- 6.Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- 7.Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- 8.Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- 9.Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- 10.DDR3 SDRAM devices supporting optional down binning to CL=7 and CL=9, and tAA/tRCD/tRP must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3-1333H devices supporting down binning to DDR3-1066F should program 13.125 ns in SPD bytes for tAamin (Byte 16), tRCdmin (Byte 18), and tRPmin (Byte 20). DDR3-1600K devices supporting down binning to DDR3-1333H or DDR3-1600F should program 13.125 ns in SPD bytes for tAamin (Byte 16), tRCdmin (Byte 18), and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accordingly. For example, 49.125ns (tRASmin + tRPmin = 36 ns + 13.125 ns) for DDR3-1333H and 48.125ns (tRASmin + tRPmin = 35 ns + 13.125 ns) for DDR3-1600K.
- 11.DDR3 SDRAM devices supporting optional down binning to CL=11, CL=9 and CL=7, tAA/tRCD/tRPmin must be 13.125ns. SPD setting must be programmed to match. For example, DDR3-1866 devices supporting down binning to DDR3-1600 or DDR3-1333 or 1066 should program 13.125ns in SPD bytes for tAamin(byte 16), tRCdmin(byte 18) and tRPmin(byte 20) is programmed to 13.125ns, tRCmin(byte 21,23) also should be programmed accordingly. For example, 47.125ns (tRASmin + tRPmin = 34ns + 13.125ns)

**12.0 Physical Dimensions: (2Gx4-DDP Based)
4Gx72 (4 Ranks)**



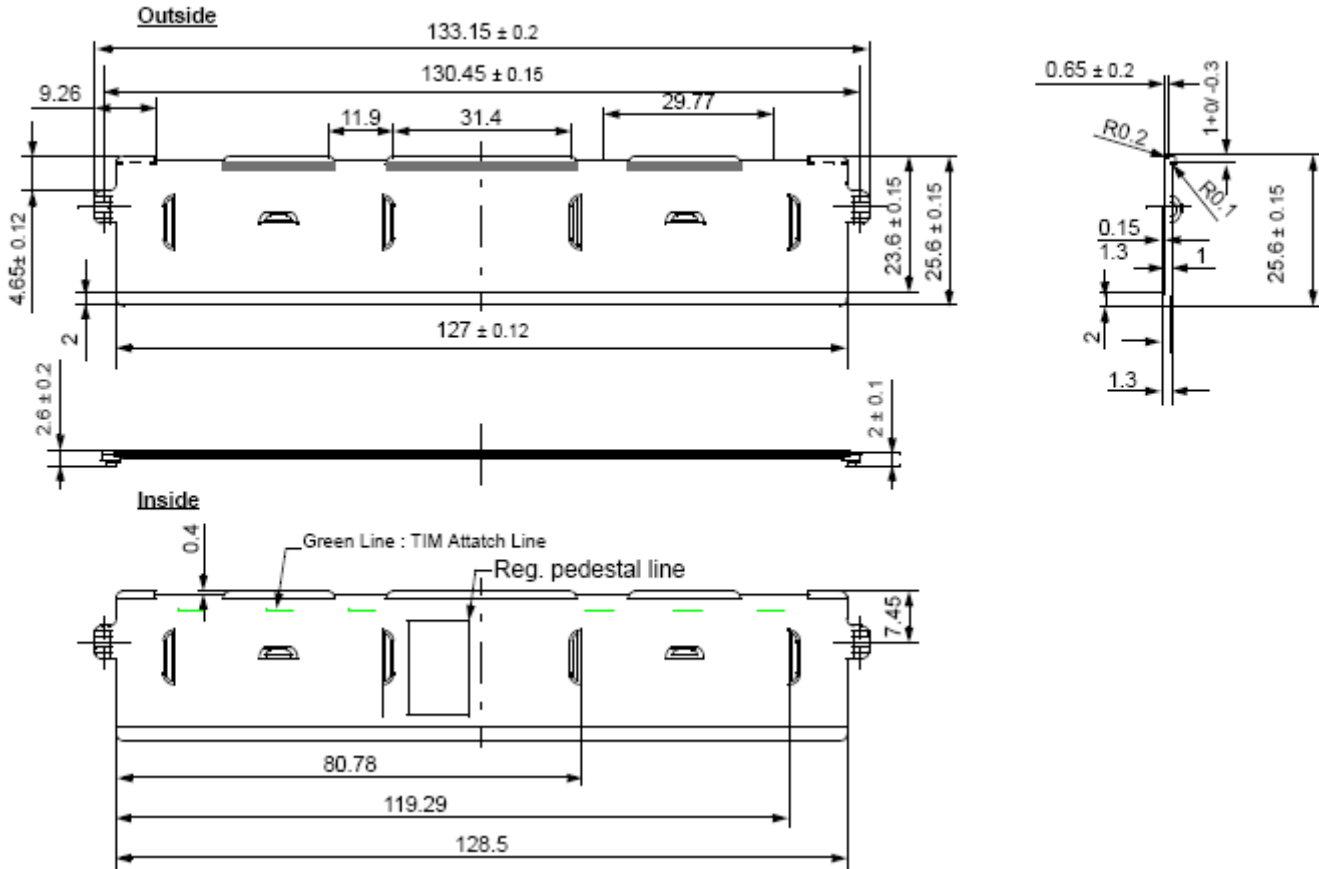
Note:

1. ±0.13 tolerance on all dimensions unless otherwise stated.

Units: millimeters

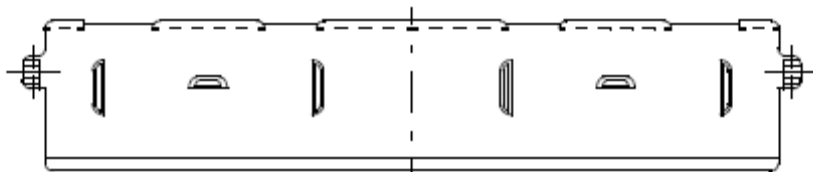
13.0 Heat Spreader

1. FRONT PART



2. BACK PART

Outside



Inside

Green Line : TIM Attach Line

