# DDR2 Unbuffered DIMM Module

## 1GB based on 512Mbit components

60 Balls TFBGA with Pb-Free


**Revision 1.0 (Mar. 2006)**
-Initial Release

## 1.0 Feature

- JEDEC standard 1.8V +/- 0.1V Power Supply
- Standard Double-Data-Rate-Two Synchronous DRAMs with single 1.8V power supply
- Programmable CAS latencies (3,4,5,6), Burst Length (4 & 8) and Burst Type
- Auto Refresh (CRB) and Self Refresh
- Bi-directional Differential Data Strobe (Single ended data strobe is option)
- Off Chip Driver (OCD) impedance adjustment
- On-Die termination with selectable values (50/75/150 ohms or disable)
- PASR (Partial Array Self Refresh)
- Average Refresh Period 7.8us at lower than a TCASE 85°C, 3.9us at 85°C < TCASE < 95 °C - support High Temperature Self-Refresh rate enable feature
- Serial presence detect with EEPROM
- DIMM Dimension (Nominal) 30.00 mm high, 133.35 mm wide
- All speed grades faster than DDR400 comply with DDR400 timing specifications
- Based on JEDEC standard reference Raw Cards Lay out.
- RoHS compliant
- Gold plated contacts

## 2.0 Ordering Information

| Part number | Density | Module Organization | Component composition | Component PKG | Module Rank | Description |
|---|---|---|---|---|---|---|
| T800UB1GV2 | 1GB | 128Mx64 | 64Mx8*16 | TFBGA | 2 | 1GB 2Rx8 PC2-6400R |

## 3.0 Operating Frequencies

| | DDR2-800 | DDR2-667 | DDR2-533 | DDR-400 | Unit |
|---|---|---|---|---|---|
| Speed @ CL3 | - | 400 | 400 | 400 | Mbps |
| Speed @ CL4 | 400 | 533 | 533 | 400 | Mbps |
| Speed @ CL5 | 533 | 667 | 533 | - | Mbps |
| Speed @ CL6 | 800 | - | - | - | Mbps |
| CL-tRCD-tRP | 6-6-6 | 5-5-5 | 4-4-4 | 3-3-3 | CK |

## 4.0 Absolute Maximum DC Rating

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| $V_{in}$ , Vout | Voltage on any pin relative to $V_{SS}$ | -0.5 ~ 2.3 | V |
| $V_{DD}$ | Voltage on $V_{DD}$ & $V_{DDQ}$ supply relative to $V_{ss}$ | -1.0 ~ 2.3 | V |
| $V_{DDQ}$ | Short circuit current | -0.5 ~ 2.3 | V |
| $V_{DDL}$ | Power dissipation | -0.5 ~ 2.3 | V |
| $T_{STG}$ | Storage Temperature | -55 ~ + 100 | °C |

## 5.0 DIMM Pin Configurations (Front side/Back side)

| Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $V_{REF}$ | 121 | $V_{SS}$ | 31 | DQ19 | 151 | $V_{SS}$ | 61 | A4 | 181 | $V_{DDQ}$ | 91 | $V_{SS}$ | 211 | DM5/DQS14 |
| 2 | $V_{SS}$ | 122 | DQ4 | 32 | $V_{SS}$ | 152 | DQ28 | 62 | $V_{DDQ}$ | 182 | A3 | 92 | $\overline{DQS}$5 | 212 | NC/$\overline{DQS}$14 |
| 3 | DQ0 | 123 | DQ5 | 33 | DQ24 | 153 | DQ29 | 63 | A2 | 183 | A1 | 93 | DQS5 | 213 | $V_{SS}$ |
| 4 | DQ1 | 124 | $V_{SS}$ | 34 | DQ25 | 154 | $V_{SS}$ | 64 | $V_{DD}$ | 184 | $V_{DD}$ | 94 | $V_{SS}$ | 214 | DQ46 |
| 5 | $V_{SS}$ | 125 | DM0/DQS9 | 35 | $V_{SS}$ | 155 | DM3/DQS12 | KEY | | | | 95 | DQ42 | 215 | DQ47 |
| 6 | $\overline{DQS}$0 | 126 | NC/$\overline{DQS}$9 | 36 | $\overline{DQS}$3 | 156 | NC/$\overline{DQS}$12 | 65 | $V_{SS}$ | 185 | CK0 | 96 | DQ43 | 216 | $V_{SS}$ |
| 7 | DQS0 | 127 | $V_{SS}$ | 37 | DQS3 | 157 | $V_{SS}$ | 66 | $V_{SS}$ | 186 | $\overline{CK0}$ | 97 | $V_{SS}$ | 217 | DQ52 |
| 8 | $V_{SS}$ | 128 | DQ6 | 38 | $V_{SS}$ | 158 | DQ30 | 67 | $V_{DD}$ | 187 | $V_{DD}$ | 98 | DQ48 | 218 | DQ53 |
| 9 | DQ2 | 129 | DQ7 | 39 | DQ26 | 159 | DQ31 | 68 | NC/Par_in | 188 | A0 | 99 | DQ99 | 219 | $V_{SS}$ |
| 10 | DQ3 | 130 | $V_{SS}$ | 40 | DQ27 | 160 | $V_{SS}$ | 69 | $V_{DD}$ | 189 | $V_{DD}$ | 100 | VSS | 220 | RFU |
| 11 | $V_{SS}$ | 131 | DQ12 | 41 | $V_{SS}$ | 161 | CB4 | 70 | A10/AP | 190 | BA1 | 101 | SA2 | 221 | RFU |
| 12 | DQ8 | 132 | DQ13 | 42 | CB0 | 162 | CB5 | 71 | BA0 | 191 | $V_{DDQ}$ | 102 | NC(Test) | 222 | $V_{SS}$ |
| 13 | DQ9 | 133 | $V_{SS}$ | 43 | CB1 | 163 | $V_{SS}$ | 72 | $V_{DDQ}$ | 192 | $\overline{RAS}$ | 103 | $V_{SS}$ | 223 | DM6/DQS15 |
| 14 | $V_{SS}$ | 134 | DM1/DQS10 | 44 | $V_{SS}$ | 164 | DM8/DQS17 | 73 | $\overline{WE}$ | 193 | S0 | 104 | $\overline{DQS}$6 | 224 | NC/$\overline{DQS}$15 |
| 15 | $\overline{DQS}$1 | 135 | NC/$\overline{DQS}$10 | 45 | $\overline{DQS}$8 | 165 | NC/$\overline{DQS}$17 | 74 | $\overline{CAS}$ | 194 | $V_{DDQ}$ | 105 | DQS6 | 225 | $V_{SS}$ |
| 16 | DQS1 | 136 | $V_{SS}$ | 46 | DQS8 | 166 | $V_{SS}$ | 75 | VDDQ | 195 | ODT0 | 106 | $V_{SS}$ | 226 | DQ54 |
| 17 | $V_{SS}$ | 137 | RFU | 47 | $V_{SS}$ | 167 | CB6 | 76 | S1 | 196 | A13 | 107 | DQ50 | 227 | DQ55 |
| 18 | $\overline{RESET}$ | 138 | RFU | 48 | CB2 | 168 | CB7 | 77 | ODT1 | 197 | $V_{DD}$ | 108 | DQ51 | 228 | $V_{SS}$ |
| 19 | NC | 139 | $V_{SS}$ | 49 | CB3 | 169 | $V_{SS}$ | 78 | $V_{DDQ}$ | 198 | $V_{SS}$ | 109 | $V_{SS}$ | 229 | DQ60 |
| 20 | $V_{SS}$ | 140 | DQ14 | 50 | $V_{SS}$ | 170 | $V_{DDQ}$ | 79 | $V_{SS}$ | 199 | DQ36 | 110 | DQ56 | 230 | DQ61 |
| 21 | DQ10 | 141 | DQ15 | 51 | $V_{DDQ}$ | 171 | CKE1 | 80 | DQ32 | 200 | DQ37 | 111 | DQ57 | 231 | $V_{SS}$ |
| 22 | DQ11 | 142 | VSS | 52 | CKE0 | 172 | $V_{DD}$ | 81 | DQ33 | 201 | $V_{SS}$ | 112 | $V_{SS}$ | 232 | DM7/DQS16 |
| 23 | $V_{SS}$ | 143 | DQ20 | 53 | $V_{DD}$ | 173 | NC | 82 | $V_{SS}$ | 202 | DM4/DQS13 | 113 | $\overline{DQS}$7 | 233 | NC/$\overline{DQS}$16 |
| 24 | DQ16 | 144 | DQ21 | 54 | NC | 174 | NC | 83 | $\overline{DQS}$4 | 203 | NC/$\overline{DQS}$13 | 114 | DQS7 | 234 | $V_{SS}$ |
| 25 | DQ17 | 145 | $V_{SS}$ | 55 | NC/Err_Out | 175 | $V_{DDQ}$ | 84 | DQS4 | 204 | $V_{SS}$ | 115 | $V_{SS}$ | 235 | DQ62 |
| 26 | $V_{SS}$ | 146 | DM2/DQS11 | 56 | $V_{DDQ}$ | 176 | A12 | 85 | $V_{SS}$ | 205 | DQ38 | 116 | DQ58 | 236 | DQ63 |
| 27 | $\overline{DQS}$2 | 147 | NC/$\overline{DQS}$11 | 57 | A11 | 177 | A9 | 86 | DQ34 | 206 | DQ39 | 117 | DQ59 | 237 | $V_{SS}$ |
| 28 | DQS2 | 148 | $V_{SS}$ | 58 | A7 | 178 | $V_{DD}$ | 87 | DQ35 | 207 | $V_{SS}$ | 118 | VSS | 238 | $V_{DD}$SPD |
| 29 | $V_{SS}$ | 149 | DQ22 | 59 | $V_{DD}$ | 179 | A8 | 88 | $V_{SS}$ | 208 | DQ44 | 119 | SDA | 239 | SA0 |
| 30 | DQ18 | 150 | DQ23 | 60 | A5 | 180 | A6 | 89 | DQ40 | 209 | DQ45 | 120 | SCL | 240 | SA1 |
| | | | | | | | | 90 | DQ41 | 210 | $V_{SS}$ | | | | |

NC = No Connect, RFU = Reserved for Future Use
1. Pin196(A13) is used for x4/x8 base Unbuffered DIMM.
2. The TEST pin is reserved for bus analysis tools and is not connected on standard memory module products (DIMMs.)

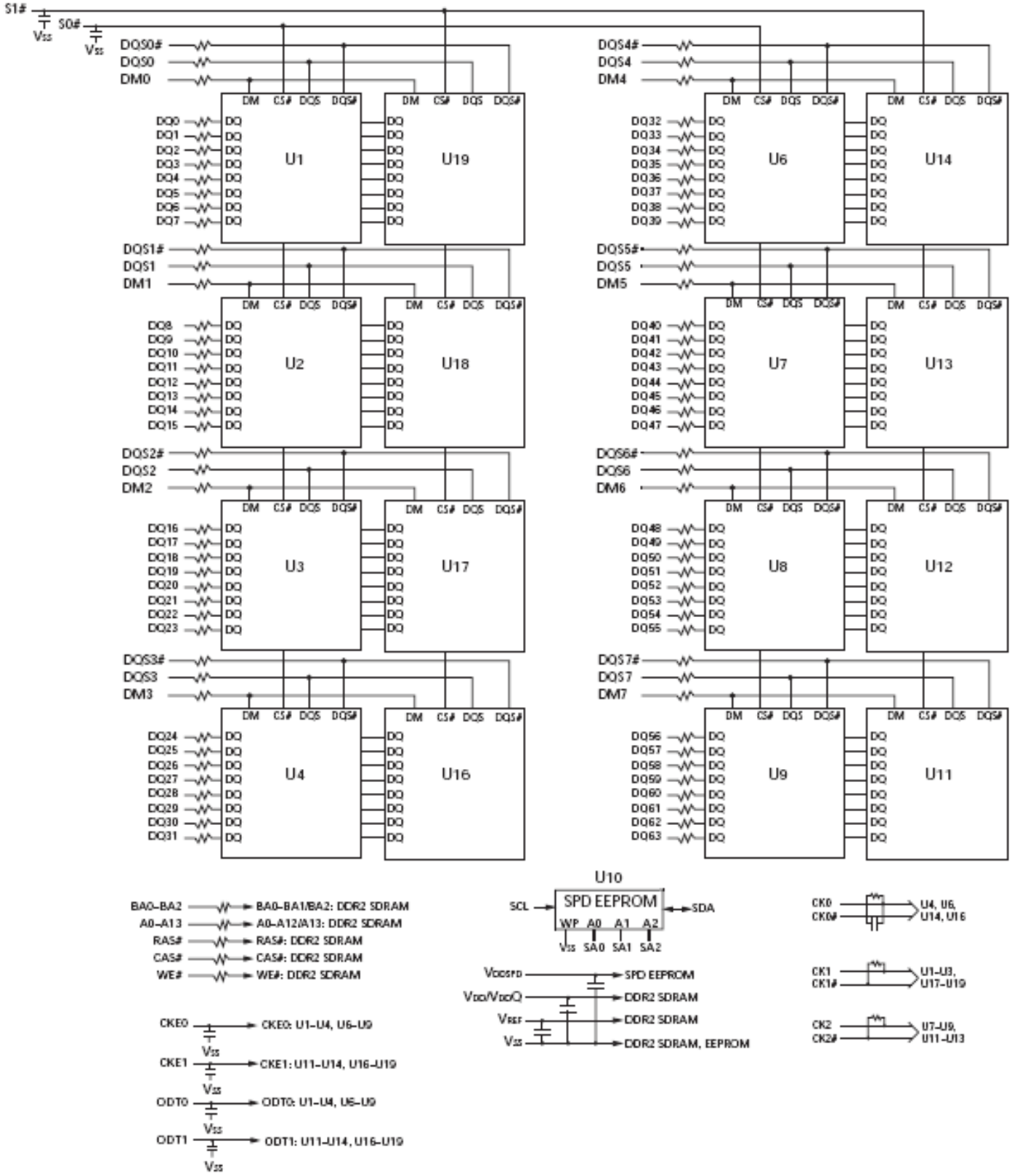
## 6.0 DIMM Pin Description

| Pin Name | Function | Pin Name | Function |
|---|---|---|---|
| A0 ~ A9, A11~A13 | Address input (Multiplexed) | ODT0~ODT1 | On Die Termination |
| A10/AP | Address Input/Auto pre-charge | CB0~CB7 | Data check bits Input/Output |
| BA0 ~ BA1 | Bank Select | DQ0~DQ63 | Data Input/Output |
| CK0 ~ CK2 | Clock (positive line of different pair) | $\overline{\text{DQS0}}$~$\overline{\text{DQS8}}$ | Data strobes, negative line |
| $\overline{\text{CK0}}$ ~ $\overline{\text{CK2}}$ | Clock (negative line of different pair) | DM(0~8), DQS(9~17) | Data Masks/Data strobes (Read) |
| CKE0, CKE1 | Clock enable input | $\overline{\text{DQS9}}$~$\overline{\text{DQS17}}$ | Data strobes (Read), negative line |
| $\overline{\text{S0}}$, $\overline{\text{S1}}$ | Chip select input | DQS0~DQS8 | Data Strobes |
| $\overline{\text{RAS}}$ | Row address strobe | RFU | Reserved for future used |
| $\overline{\text{CAS}}$ | Column address strobe | NC | No connection |
| $\overline{\text{WE}}$ | Write Enable | TEST | Memory bus test tool |
| SCL | SPD Clock Input | $V_{DD}$ | Core Power |
| SDA | SPD Data Input/Output | $V_{DDQ}$ | I/O Power |
| SA0~SA2 | SPD Address | $V_{SS}$ | Ground |
| Par_In | Parity bit for address & Control bus | $V_{REF}$ | Input/Output Reference |
| Err_Out | Parity error found in the Address and Control bus | $V_{DDSPD}$ | Serial EEPROM positive power supply |
| $\overline{\text{Reset}}$ | Register and PLL control pin | | |

## 7.0 Address Configuration

| Organization | Row Address | Column Address | Bank Address | Auto Pre-charge |
|---|---|---|---|---|
| 64Mx8(512Mb) base | A0-A13 | A0-A9 | BA0-BA1 | A10 |

## 8.0 Functional Block Diagram: 1GB, 128Mx64 Module (Populated as 2 ranks of x8 SDRAM DDR2 Module)



## 9.0 AC & DC Operating Conditions

Recommended operating conditions (Voltage referenced to Vss=0V, TA=0 to 70°C)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 1.7 | 1.8 | 1.9 | V |
| $V_{DDL}$ | Supply Voltage for DLL | 1.7 | 1.8 | 1.9 | V |
| $V_{DDQ}$ | Supply Voltage for Output | 1.7 | 1.8 | 1.9 | V |
| $V_{REF}$ | Input Reference Voltage | 0.49*$V_{DDQ}$ | 0.50*$V_{DDQ}$ | 0.51*$V_{DDQ}$ | mV |
| $V_{TT}$ | Termination Voltage | $V_{REF}$-0.04 | $V_{REF}$ | $V_{REF}$+0.04 | V |

## 10.0 Capacitance(Max.)

| Symbol | Parameter/Condition | Min | Max | Unit |
|---|---|---|---|---|
| CCK | Input capacitance, CK and $\overline{CK}$ | - | 11 | pF |
| CI1 | Input capacitance, CKE and $\overline{CS}$ | - | 12 | pF |
| CI2 | Input capacitance, Addr, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | - | 12 | pF |
| CIO | Input capacitance, DQ, DM, DQS, $\overline{DQS}$ | - | 10 | pF |

## 11.0 AC Timing Parameters & Specifications

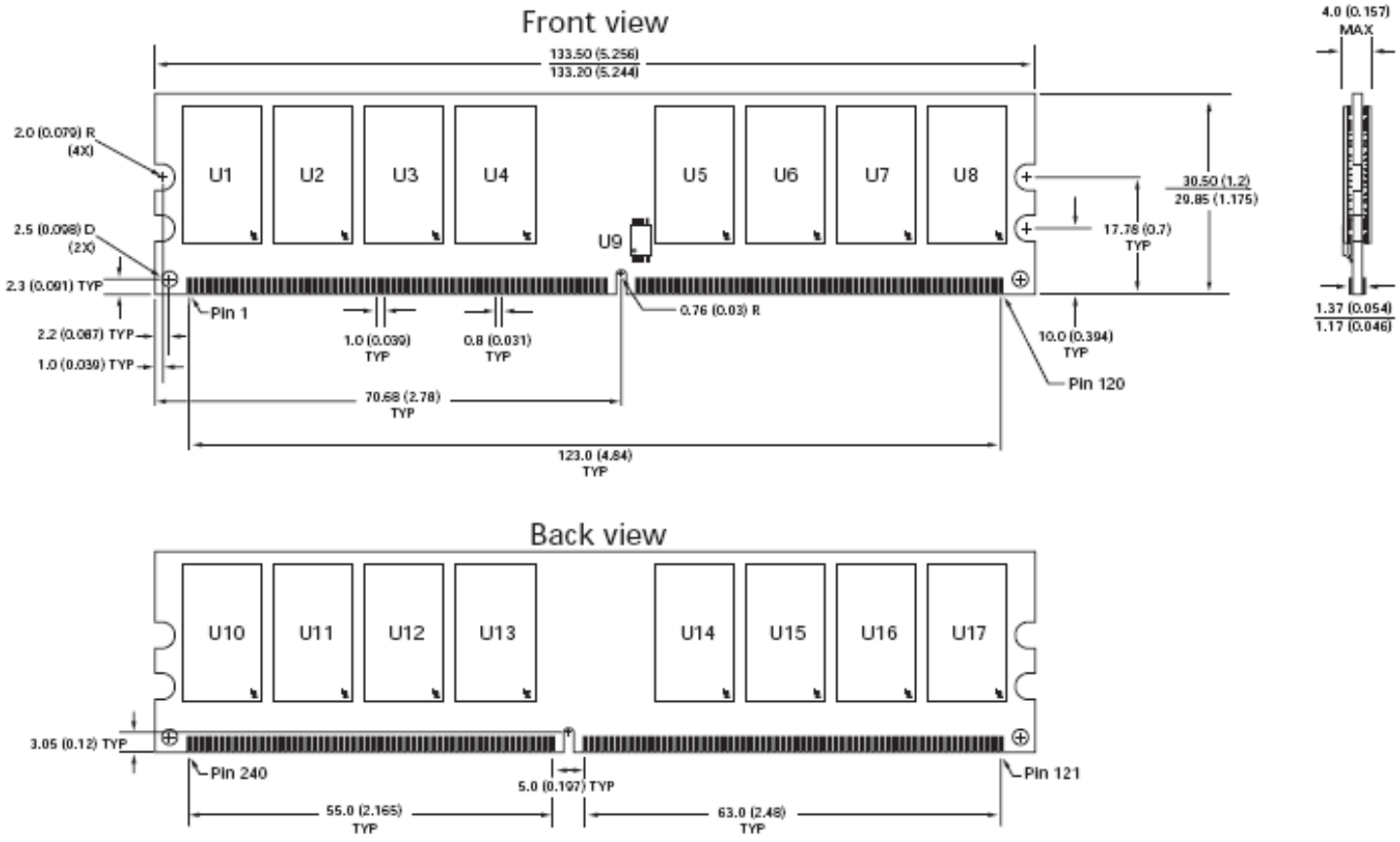
(AC operating conditions unless otherwise noted)

| Parameter | Symbol | DDR2-800 | | DDR2-667 | | DDR2-533 | | DDR2-400 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | min | max | |
| DQ output access time from CK/$\overline{CK}$ | tAC | - 400 | +400 | -450 | +450 | -500 | +500 | -600 | +600 | ps |
| DQS output access time from CK/$\overline{CK}$ | tDQSCK | -350 | +350 | -400 | +400 | -450 | +450 | -500 | +500 | ps |
| CK high-level width | tCH | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK |
| CK low-level width | tCL | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK |
| CK half period | tHP | min(tCL, tCH) | x | min(tCL, tCH | x | min(tCL, tCH | x | min(tCL, tCH | x | ps |
| Clock cycle time, CL=x | tCK | 2500 | 8000 | 3000 | 8000 | 3750 | 8000 | 5000 | 8000 | ps |
| DQ and DM input hold time | tDH(base) | 125 | x | 175 | x | 225 | x | 275 | x | ps |
| DQ and DM input setup time | tDS(base) | 50 | x | 100 | x | 100 | x | 150 | x | ps |
| Control & Address input pulse width for each input | tIPW | 0.6 | x | 0.6 | x | 0.6 | x | 0.6 | x | tCK |
| DQ and DM input pulse width for each input | tDIPW | 0.35 | x | 0.35 | x | 0.35 | x | 0.35 | x | tCK |
| Data-out high-impedance time from CK/$\overline{CK}$ | tHZ | x | tAC max | x | tAC max | x | tAC max | x | tAC max | ps |
| DQS low-impedance time from CK/$\overline{CK}$ | tLZ(DQS) | tAC min | tAC max | tAC min | tAC max | tAC min | tAC max | tAC min | tAC max | ps |
| DQ low-impedance time from CK/$\overline{CK}$ | tLZ(DQ) | 2*tAC min | tAC max | 2*tAC min | tAC max | 2*tAC min | tAC max | 2*tAC min | tAC max | ps |
| DQS-DQ skew for DQS and associated DQ signals | tDQSQ | x | 200 | x | 240 | x | 300 | x | 350 | ps |
| DQ hold skew factor | tQHS | x | 300 | x | 340 | x | 400 | x | 450 | ps |
| DQ/DQS output hold time from DQS | tQH | tHP - tQHS | x | tHP - tQHS | x | tHP - tQHS | x | tHP - tQHS | x | ps |
| First DQS latching transition to associated clock edge | tDQSS | -0.25 | 0.25 | -0.25 | 0.25 | -0.25 | 0.25 | -0.25 | 0.25 | tCK |
| DQS input high pulse width | tDQSH | 0.35 | x | 0.35 | x | 0.35 | x | 0.35 | x | tCK |
| DQS input low pulse width | tDQSL | 0.35 | x | 0.35 | x | 0.35 | x | 0.35 | x | tCK |
| DQS falling edge to CK setup time | tDSS | 0.2 | x | 0.2 | x | 0.2 | x | 0.2 | x | tCK |
| DQS falling edge hold time from CK | tDSH | 0.2 | x | 0.2 | x | 0.2 | x | 0.2 | x | tCK |
| Mode register set command cycle time | tMRD | 2 | x | 2 | x | 2 | x | 2 | x | tCK |

| Parameter | Symbol | DDR2-800 | | DDR2-667 | | DDR2-533 | | DDR2-400 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | min | max | |
| Write postamble | tWPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK |
| Write preamble | tWPRE | 0.35 | x | 0.35 | x | 0.35 | x | 0.35 | x | tCK |
| Address and control input hold time | tIH(base) | 250 | x | 275 | x | 375 | x | 475 | x | ps |
| Address and control input setup time | tIS(base) | 175 | x | 200 | x | 250 | x | 350 | x | ps |
| Read preamble | tRPRE | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | tCK |
| Read postamble | tRPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK |
| Active to active command period for 1KB page size products | tRRD | 7.5 | x | 7.5 | x | 7.5 | x | 7.5 | x | ns |
| Active to active command period for 2KB page size products | tRRD | 10 | x | 10 | x | 10 | x | 10 | x | ns |
| Four Activate Window for 1KB page size product | tFAW | 35 | | 37.5 | | 37.5 | | 37.5 | | ns |
| Four Activate Window for 2KB page size products | tFAW | 45 | | 50 | | 50 | | 50 | | ns |
| $\overline{CAS}$ to $\overline{CAS}$ command delay | tCCD | 2 | x | 2 | | 2 | | 2 | | tCK |
| Write recovery time | tWR | 15 | x | 15 | x | 15 | x | 15 | x | ns |
| Auto pre-charge write recovery + pre-charge time | tDAL | WR+tRP | x | WR+tRP | x | WR+tRP | x | WR+tRP | x | tCK |
| Internal write to read command delay | tWTR | 7.5 | | 7.5 | x | 7.5 | x | 10 | x | ns |
| Internal read to pre-charge command delay | tRTP | 7.5 | | 7.5 | | 7.5 | | 7.5 | | ns |
| Exit self refresh to a non-read command | tXSNRt | tRFC + 10 | | tRFC + 10 | | tRFC + 10 | | tRFC + 10 | | ns |
| Exit self refresh to a read command | tXSRD | 200 | | 200 | | 200 | | 200 | | tCK |
| Exit pre-charge power down to any non-read command | tXP | 2 | x | 2 | x | 2 | x | 2 | x | tCK |
| Exit active power down to read command | tXARD | 2 | x | 2 | x | 2 | x | 2 | x | tCK |
| Exit active power down to read command (slow exit, lower power) | tXARDS | 8 - AL | | 7 - AL | | 6 - AL | | 6 - AL | | tCK |
| CKE minimum pulse width (high and low pulse width) | tCKE | 3 | | 3 | | 3 | | 3 | | tCK |
| ODT turn-on delay | tAOND | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | tCK |
| ODT turn-on | tAON | tAC (min) | tAC(max) + 0.7 | tAC (min) | tAC(max)+0.7 | tAC (min) | tAC (max)+1t | tAC (min) | tAC(max) +1t | ns |
| ODT turn-on(Power-Down mode) | tAONPD | tAC (min)+2 | 2tCK+tAC (max)+1 | tAC (min)+2 | 2tCK+tAC (max)+1 | tAC (min)+2 | 2tCK +tAC (max)+1 | tAC (min)+2 | 2tCK+tAC (max)+1 | ns |
| ODT turn-off delay | tAOFD | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | tCK |
| ODT turn-off | tAOF | tAC (min) | tAC(max) + 0.6 | tAC (min) | tAC(max)+ 0.6 | tAC (min) | tAC(max) + 0.6 | tAC (min) | tAC(max) + 0.6 | ns |
| ODT turn-off (Power-Down mode) | tAOFPD | tAC (min)+2 | 2.5tCK+ tAC(max) +1 | tAC (min)+2 | 2.5tCK+ tAC(max)+1 | tAC (min)+2 | 2.5tCK+ tAC(max) +1 | tAC (min)+2 | 2.5tCK+t AC(max)+ 1 | ns |
| ODT to power down entry latency | tANPD | 3 | | 3 | | 3 | | 3 | | tCK |
| ODT power down exit latency | tAXPD | 8 | | 8 | | 8 | | 8 | | tCK |
| OCD drive mode output delay | tOIT | 0 | 12 | 0 | 12 | 0 | 12 | 0 | 12 | ns |
| Minimum time clocks remains ON after CKE asynchronously drops LOW | tDelay | tIS+tCK +tIH | | tIS+tCK +tIH | | tIS+tCK +tIH | | tIS+tCK +tIH | | ns |

## 12.0 Physical Dimensions: (64Mx8 Based)
## 128Mx64 (2 ranks)

Units : Millimeters




Tolerances :± 0.005(.13) unless otherwise specified