

# **DDR2 SODIMM Module**

**2GB based on 1Gbit component**

**60 Balls FBGA with Pb-Free**



**Revision 1.0 (Mar. 2006)**  
-Initial Release

**1.0 Feature**

- JEDEC standard 1.8V +/- 0.1V Power Supply
- VDDQ = 1.8V ± 0.1V
- 200 MHz fCK for 400Mb/sec/pin, 267MHz fCK for 533Mb/sec/pin, 333MHz fCK for 667Mb/sec/pin, 400MHz fCK for 800Mb/sec/pin
- 4 Banks
- Posted CAS
- Programmable CAS Latency: 3, 4, 5
- Programmable Additive Latency: 0, 1, 2, 3 and 4
- Write Latency (WL) = Read Latency (RL) –1
- Burst Length: 4, 8(Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver (OCD) Impedance Adjustment
- On Die Termination with selectable values 50/75/150 ohms or disable)
- PASR Partial Array Self Refresh)
- Average Refresh Period 7.8us at lower than a TCASE 85°C, 3.9us at 85°C < TCASE < 95 °C- support High Temperature Self-Refresh rate enable feature
- Package: 60ball FBGA - 128Mx8
- All of Lead-free products are compliant for RoHS
- Gold plated contacts

**2.0 Ordering Information**

Part number	Density	Module Organization	Component composition	Component PKG	Module Rank	Description
T800SB2G/H	2GB	256Mx64	128Mx8*16	FBGA	2	2GB 2Rx8 PC2-6400R

**3.0 Operating Frequencies**

	DDR2-800	DDR2-667	DDR2-533	DDR-400	Unit
Speed @ CL3	400	400	400	400	Mbps
Speed @ CL4	533	533	533	400	Mbps
Speed @ CL5	800	667	533	-	Mbps
CL-tRCD-tRP	5-5-5	5-5-5	4-4-4	3-3-3	CK

**4.0 Absolute Maximum DC Rating**

Symbol	Parameter	Rating	Units
V <sub>in</sub> , V <sub>out</sub>	Voltage on any pin relative to V <sub>SS</sub>	-0.5 ~ 2.3	V
V <sub>DD</sub>	Voltage on V <sub>DD</sub> & V <sub>DDQ</sub> supply relative to V <sub>SS</sub>	-1.0 ~ 2.3	V
V <sub>DDQ</sub>	Short circuit current	-0.5 ~ 2.3	V
V <sub>DDL</sub>	Power dissipation	-0.5 ~ 2.3	V
T <sub>STG</sub>	Storage Temperature	-55 ~ + 100	°C

**5.0 DIMM Pin Configurations (Front side/Back side)**

Pin	Front	Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back	Pin	Back
1	V <sub>REF</sub>	51	DQS2	101	A1	151	DQ42	2	V <sub>SS</sub>	52	DM2	102	A0	152	DQ46
3	V <sub>SS</sub>	53	V <sub>SS</sub>	103	V <sub>DD</sub>	153	DQ43	4	DQ4	54	V <sub>SS</sub>	104	V <sub>DD</sub>	154	DQ47
5	DQ0	55	DQ18	105	A10/AP	155	V <sub>SS</sub>	6	DQ5	56	DQ22	106	BA1	156	V <sub>SS</sub>
7	DQ1	57	DQ19	107	BA0	157	DQ48	8	V <sub>SS</sub>	58	DQ23	108	RAS#	158	DQ52
9	V <sub>SS</sub>	59	V <sub>SS</sub>	109	WE#	159	DQ49	10	DM0	60	V <sub>SS</sub>	110	S0#	160	DQ53
11	DQS0#	61	DQ24	111	V <sub>DD</sub>	161	V <sub>SS</sub>	12	V <sub>SS</sub>	62	DQ28	112	V <sub>DD</sub>	162	V <sub>SS</sub>
13	DQS0	63	DQ25	113	CAS#	163	NC	14	DQ6	64	DQ29	114	ODT0	164	CK1
15	V <sub>SS</sub>	65	V <sub>SS</sub>	115	NC/S1#	165	V <sub>SS</sub>	16	DQ7	66	V <sub>SS</sub>	116	A13	166	CK1#
17	DQ2	67	DM3	117	V <sub>DD</sub>	167	DQS6#	18	V <sub>SS</sub>	68	DQS3#	118	V <sub>DD</sub>	168	V <sub>SS</sub>
19	DQ3	69	NC	119	ODT1	169	DQS6	20	DQ12	70	DQS3	120	NC	170	DM6
21	V <sub>SS</sub>	71	V <sub>SS</sub>	121	V <sub>SS</sub>	171	V <sub>SS</sub>	22	DQ13	72	V <sub>SS</sub>	122	V <sub>SS</sub>	172	V <sub>SS</sub>
23	DQ8	73	DQ26	123	DQ32	173	DQ50	24	V <sub>SS</sub>	74	DQ30	124	DQ36	174	DQ54
25	DQ9	75	DQ27	125	DQ33	175	DQ51	26	DM1	76	DQ31	126	DQ37	176	DQ55
27	V <sub>SS</sub>	77	V <sub>SS</sub>	127	V <sub>SS</sub>	177	V <sub>SS</sub>	28	V <sub>SS</sub>	78	V <sub>SS</sub>	128	V <sub>SS</sub>	178	V <sub>SS</sub>
29	DQS1#	79	CKE0	129	DQS4#	179	DQ56	30	CK0	80	CKE1	130	DM4	180	DQ60
31	DQS1	81	V <sub>DD</sub>	131	DQS4	181	DQ57	32	CK0#	82	V <sub>DD</sub>	132	V <sub>SS</sub>	182	DQ61
33	V <sub>SS</sub>	83	NC	133	V <sub>SS</sub>	183	V <sub>SS</sub>	34	V <sub>SS</sub>	84	NC	134	DQ38	184	V <sub>SS</sub>
35	DQ10	85	BA2	135	DQ34	185	DM7	36	DQ14	86	NC	136	DQ39	186	DQS7#
37	DQ11	87	V <sub>DD</sub>	137	DQ35	187	V <sub>SS</sub>	38	DQ15	88	V <sub>DD</sub>	138	V <sub>SS</sub>	188	DQS7
39	V <sub>SS</sub>	89	A12	139	V <sub>SS</sub>	189	DQ58	40	V <sub>SS</sub>	90	A11	140	DQ44	190	V <sub>SS</sub>
41	V <sub>SS</sub>	91	A9	141	DQ40	191	DQ59	42	V <sub>SS</sub>	92	A7	142	DQ45	192	DQ62
43	DQ16	93	A8	143	DQ41	193	V <sub>SS</sub>	44	DQ20	94	A6	144	V <sub>SS</sub>	194	DQ63
45	DQ17	95	V <sub>DD</sub>	145	V <sub>SS</sub>	195	SDA	46	DQ21	96	V <sub>DD</sub>	146	DQS5#	196	V <sub>SS</sub>
47	V <sub>SS</sub>	97	A5	147	DM5	197	SCL	48	V <sub>SS</sub>	98	A4	148	DQS5	198	SA0
49	DQS2#	99	A3	149	V <sub>SS</sub>	199	V <sub>DD</sub> SPD	50	NC	100	A2	150	V <sub>SS</sub>	200	SA1

**6.0 Dimm Pin Description**

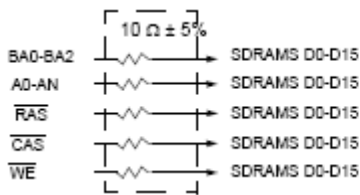
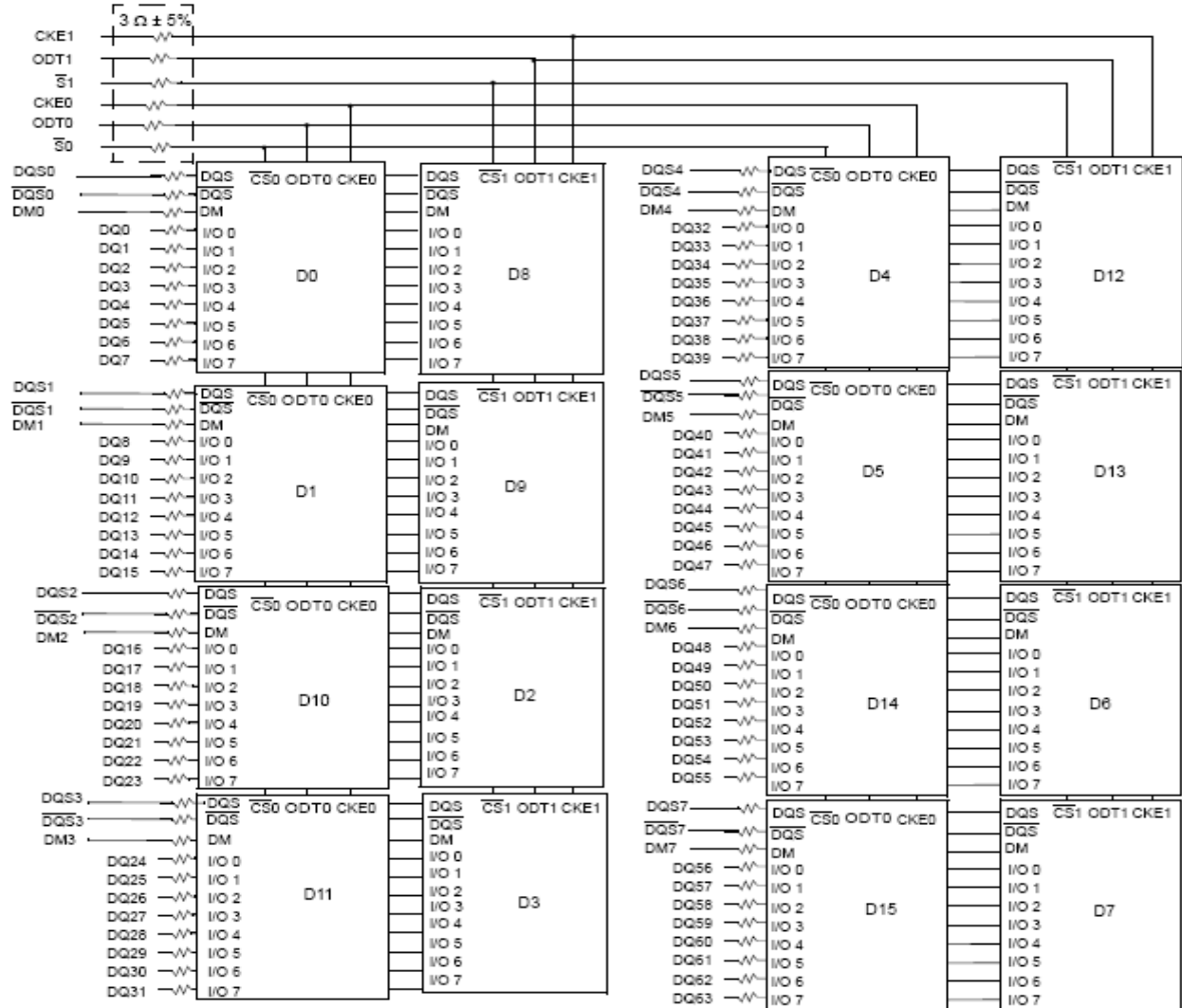
Pin Name	Function	Pin Name	Function
A0 ~ A9, A11 ~ A13	Address input (Multiplexed)	ODT0~ODT1	On Die Termination
A10/AP	Address Input/Auto pre-charge	DQ0~DQ63	Data Input/Output
BA0 ~ BA1, BA2	Bank Select	CK0# ~ CK1#	Clock input, negative line
CK0 ~ CK1	Clock input	DM0 ~ DM7	Data Masks/Data strobes (Read)
CKE0, CKE1	Clock enable input	DQS0~DQS7	Data Strobes
S0#, S1#	Chip select input	DQS0#~DQS7#	Data strobes, negative line
RAS#	Row address strobe	V <sub>DD</sub>	Core Power
CAS#	Column address strobe	V <sub>REF</sub>	Input/Output Reference
WE#	Write Enable	V <sub>SS</sub>	Ground
SCL	SPD Clock Input	V <sub>DDSPD</sub>	SPD
SDA	SPD Data Input/Output	NC	No connection
SA0~SA1	SPD Address		

**7.0 Address Configuration**

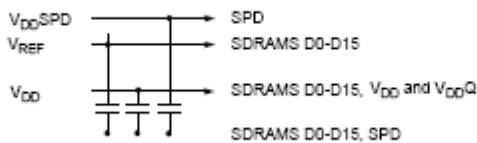
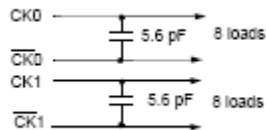
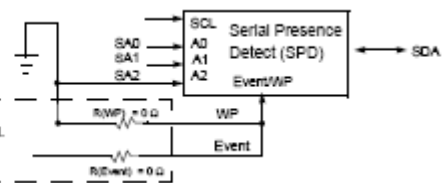
Organization	Row Address	Column Address	Bank Address	Auto Precharge
128Mx8(1Gb) base	A0-A13	A0-A9	BA0-BA2	A10

**8.0 Functional Block Diagram: 2GB, 256Mx64 Module**

(Populated as 2 ranks of x8 SDRAM DDR2 Module)



Note:  
For normal operation only R(WP) is placed.  
For the SPD temperature sensor option only R(Event) is placed.



#Unless otherwise noted, resistor values are  $22 \Omega \pm 5\%$  DQ wiring may differ from that described in this drawing; described in this drawing; however, DQ/DM/DQS/DQS relationships are maintained as shown

**9.0 AC & DC Operating Conditions**

Recommended operating conditions (Voltage referenced to V<sub>SS</sub>=0V, TA=0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>DD</sub>	Supply Voltage	1.7	1.8	1.9	V
V <sub>DDL</sub>	Supply Voltage for DLL	1.7	1.8	1.9	V
V <sub>DDQ</sub>	Supply Voltage for Output	1.7	1.8	1.9	V
V <sub>REF</sub>	Input Reference Voltage	0.49*V <sub>DDQ</sub>	0.50*V <sub>DDQ</sub>	0.51*V <sub>DDQ</sub>	mV
V <sub>TT</sub>	Termination Voltage	V <sub>REF</sub> -0.04	V <sub>REF</sub>	V <sub>REF</sub> +0.04	V

**10.0 AC Timing Parameters & Specifications**

(AC operating conditions unless otherwise noted)

Parameter	Symbol	DDR2-800		DDR2-667		DDR2-533		DDR2-400		Units
		min	max	min	max	min	max	min	max	
DQ output access time from CK/ $\overline{\text{CK}}$	t <sub>AC</sub>	-400	+400	-450	+450	-500	+500	-600	+600	ps
DQS output access time from CK/CK	t <sub>DQ<sub>SCK</sub></sub>	-350	+350	-400	+400	-450	+450	-500	+500	ps
CK high-level width	t <sub>CH</sub>	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
CK low-level width	t <sub>CL</sub>	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
CK half period	t <sub>HP</sub>	min(t <sub>CL</sub> , t <sub>CH</sub> )	x	min(t <sub>CL</sub> , t <sub>CH</sub> )	x	min(t <sub>CL</sub> , t <sub>CH</sub> )	x	min(t <sub>CL</sub> , t <sub>CH</sub> )	x	ps
Clock cycle time, CL=x	t <sub>CK</sub>	2500	8000	3000	8000	3750	8000	5000	8000	ps
DQ and DM input hold time	t <sub>DH(base)</sub>	125	x	175	x	225	x	275	x	ps
DQ and DM input setup time	t <sub>DS(base)</sub>	50	x	100	x	100	x	150	x	ps
Control & Address input pulse width for each input	t <sub>IPW</sub>	0.6	x	0.6	x	0.6	x	0.6	x	tCK
DQ and DM input pulse width for each input	t <sub>DIPW</sub>	0.35	x	0.35	x	0.35	x	0.35	x	tCK
Data-out high-impedance time from CK/CK	t <sub>HZ</sub>	x	t <sub>AC max</sub>	x	t <sub>AC max</sub>	x	t <sub>AC max</sub>	x	t <sub>AC max</sub>	ps
DQS low-impedance time from CK/CK	t <sub>LZ(DQS)</sub>	t <sub>AC min</sub>	t <sub>AC max</sub>	t <sub>AC min</sub>	t <sub>AC max</sub>	t <sub>AC min</sub>	t <sub>AC max</sub>	t <sub>AC min</sub>	t <sub>AC max</sub>	ps
DQ low-impedance time from CK/CK	t <sub>LZ(DQ)</sub>	2*t <sub>AC min</sub>	t <sub>AC max</sub>	2*t <sub>AC min</sub>	t <sub>AC max</sub>	2*t <sub>AC min</sub>	t <sub>AC max</sub>	2*t <sub>AC min</sub>	t <sub>AC max</sub>	ps
DQS-DQ skew for DQS and associated DQ signals	t <sub>DQSQ</sub>	x	200	x	240	x	300	x	350	ps
DQ hold skew factor	t <sub>QHS</sub>	x	300	x	340	x	400	x	450	ps
DQ/DQS output hold time from DQS	t <sub>QH</sub>	t <sub>HP</sub> - t <sub>QHS</sub>	x	t <sub>HP</sub> - t <sub>QHS</sub>	x	t <sub>HP</sub> - t <sub>QHS</sub>	x	t <sub>HP</sub> - t <sub>QHS</sub>	x	ps
First DQS latching transition to associated clock edge	t <sub>DQSS</sub>	-0.25	0.25	-0.25	0.25	-0.25	0.25	-0.25	0.25	tCK
DQS input high pulse width	t <sub>DQSH</sub>	0.35	x	0.35	x	0.35	x	0.35	x	tCK
DQS input low pulse width	t <sub>DQSL</sub>	0.35	x	0.35	x	0.35	x	0.35	x	tCK
DQS falling edge to CK setup time	t <sub>DSS</sub>	0.2	x	0.2	x	0.2	x	0.2	x	tCK
DQS falling edge hold time from CK	t <sub>DSH</sub>	0.2	x	0.2	x	0.2	x	0.2	x	tCK
Mode register set command cycle time	t <sub>MRD</sub>	2	x	2	x	2	x	2	x	tCK
Write postamble	t <sub>WPST</sub>	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Write preamble	t <sub>WPRE</sub>	0.35	x	0.35	x	0.35	x	0.35	x	tCK

**200-Pin SODIMM**

**DDR2 SDRAM**

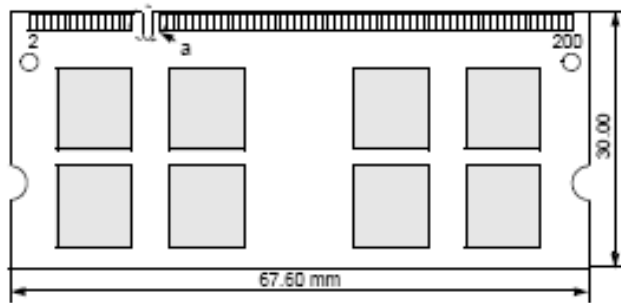
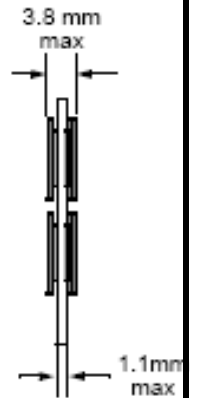
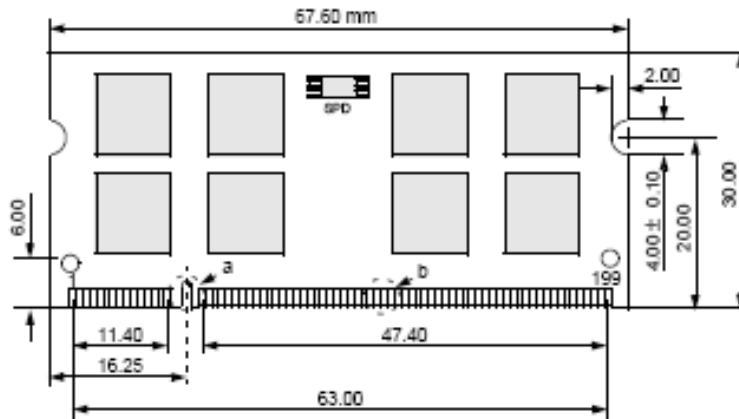
Parameter	Symbol	DDR2-800		DDR2-667		DDR2-533		DDR2-400		Units
		min	max	min	max	min	max	min	max	
Address and control input hold time	tIH(base)	250	x	275	x	375	x	475	x	ps
Address and control input setup time	tIS(base)	175	x	200	x	250	x	350	x	ps
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Active to active command period for 1KB page size products	tRRD	7.5	x	7.5	x	7.5	x	7.5	x	ns
Active to active command period for 2KB page size products	tRRD	10	x	10	x	10	x	10	x	ns
Four Activate Window for 1KB page size products	tFAW	35		37.5		37.5		37.5		ns
Four Activate Window for 2KB page size products	tFAW	45		50		50		50		ns
CAS to CAS command delay	tCCD	2	x	2		2		2		tCK
Write recovery time	tWR	15	x	15	x	15	x	15	x	ns
Auto precharge write recovery + precharge time	tDAL	WR+tRP	x	WR+tRP	x	WR+tRP	x	WR+tRP	x	tCK
Internal write to read command delay	tWTR	7.5		7.5	x	7.5	x	10	x	ns
Internal read to precharge command delay	tRTP	7.5		7.5		7.5		7.5		ns
Exit self refresh to a non-read command	tXSNRt	tRFC + 10		tRFC + 10		tRFC + 10		tRFC + 10		ns
Exit self refresh to a read command	tXSRD	200		200		200		200		tCK
Exit precharge power down to any non-read command	tXP	2	x	2	x	2	x	2	x	tCK
Exit active power down to read command	tXARD	2	x	2	x	2	x	2	x	tCK
Exit active power down to read command (slow exit, lower power)	tXARDS	8 - AL		7 - AL		6 - AL		6 - AL		tCK
CKE minimum pulse width (high and low pulse width)	tCKE	3		3		3		3		tCK
ODT turn-on delay	tAOND	2	2	2	2	2	2	2	2	tCK
ODT turn-on	tAON	tAC(min)	tAC(max) + 0.7	tAC(min)	tAC(max)+0.7	tAC(min)	tAC(max) + 1t	tAC(min)	tAC(max) + 1t	ns
ODT turn-on (Power-Down mode)	tAONPD	tAC(min) + 2	2tCK + tAC (max)+1	tAC(min) + 2	2tCK + tAC(max)+1	tAC(min) + 2	2tCK + tAC (max)+1	tAC(min) + 2	2tCK + tAC (max)+1	ns
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	tCK
ODT turn-off	tAOF	tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max)+ 0.6	tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	ns
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min) + 2	2.5tCK + tAC (max)+1	tAC(min) + 2	2.5tCK + tAC(max)+1	tAC(min) + 2	2.5tCK + Tac (max)+1	tAC(min) + 2	2.5tCK + tAC (max)+1	ns
ODT to power down entry latency	tANPD	3		3		3		3		tCK
ODT power down exit latency	tAXPD	8		8		8		8		tCK
OCD drive mode output delay	tOIT	0	12	0	12	0	12	0	12	ns
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tC K + tIH		tIS+tC K + tIH		tIS+tC K + tIH		tIS+tC K + tIH		ns

**200-Pin SODIMM**

**DDR2 SDRAM**

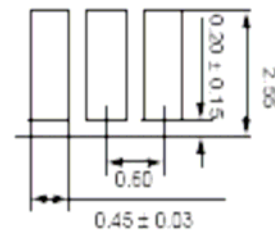
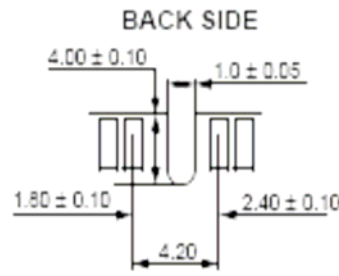
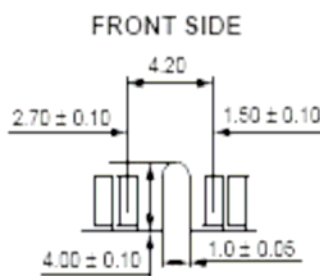
**11.0 Physical Dimensions: (128Mx8 Based)  
256Mx64 (2 Ranks)**

Units : Millimeters



DETAIL a

DETAIL b



Tolerances : ± 0.005(.13) unless otherwise specified