DDR2 SODIMM Module

256MB based on 256Mbit component

256MB, 512MB and 1GB based on 512Mbit component

1GB and 2GB based on 1Gbit component

60 Balls & 84 Balls FBGA with Pb-Free

Revision 1.0 (Mar. 2006)
-Initial Release

1.0 Feature

- JEDEC standard 1.8V +/- 0.1V Power Supply
- VDDQ = 1.8V ± 0.1V
- 200 MHz fCK for 400Mb/sec/pin, 267MHz fCK for 533Mb/sec/pin, 333MHz fCK for 667Mb/sec/pin, 400MHz fCK for 800Mb/sec/pin
- 4 Banks
- Posted CAS
- Programmable CAS Latency: 3, 4, 5
- Programmable Additive Latency: 0, 1 , 2 , 3 and 4
- Write Latency(WL) = Read Latency(RL) –1
- Burst Length: 4 , 8(Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- On Die Termination with selectable values(50/75/150 ohms or disable)
- PASR(Partial Array Self Refresh)
- Average Refresh Period 7.8us at lower than a TCASE 85°C, 3.9us at 85°C < TCASE < 95 °C- support High Temperature Self-Refresh rate enable feature
- Package: 60ball FBGA - 64Mx8 , 84ball FBGA - 32Mx16
- All of Lead-free products are compliant for RoHS
- Gold plated contacts

2.0 Ordering Information

Part Number	Density	Module Org	Description / CL	DRAM Configuration/Components
	400 MHz	PC3200		
T400SC256	256MB	32M x 64	1 Bank, 3	32M x 8 (8 pcs)
T400SB1G_E	512MB	128M x 64	2 Bank, 3	64M x 8 (16 pcs)
T400SC512	512MB	64M x 64	1 Bank, 3	64M x 8 (8 pcs)
T400SC512E	512MB	64M x 64	1 Bank, 3	64M x 8 (8 pcs)
T400SB1G	1GB	128M x 64	2 Bank, 3	64M x 8 (16 pcs)
	533 MHz	PC4300		
T533SC256	256MB	32M x 64	1 Bank, 4	32M x 8 (8 pcs)
T533SC512	512MB	64M x 64	1 Bank, 4	64M x 8 (8 pcs)
T533SC512E	512MB	64M x 64	1 Bank, 4	64M x 8 (8 pcs)
T533SB1G	1GB	128M x 64	2 Bank, 4	64M x 8 (16 pcs)
T533SB1G_E	1GB	128M x 64	2 Bank, 4	64M x 8 (16 pcs)
T533SB1G_S	1GB	128M x 64	2 Bank, 4	64M x 8 (16 pcs)
	667MHz	PC5300		
T667SC512	512MB	64M x 64	1 Bank, 5	64M x 8 (8 pcs)
T667SC512E	512MB	64M x 64	1 Bank, 5	64M x 8 (8 pcs)
T667SB1G	1GB	128M x 64	2 Bank, 5	64M x 8 (16 pcs)
T667SB1G_E	1GB	128M x 64	2 Bank, 5	64M x 8 (16 pcs)
T667SB2G_M	2GB	256M x 64	2 Bank, 5	128M x 8 (16 pcs)

3.0 Operating Frequencies

	DDR2-800	DDR2-667	DDR2-533	DDR-400	Unit
Speed @ CL3	400	400	400	400	Mbps
Speed @ CL4	533	533	533	400	Mbps
Speed @ CL5	800	667	533	-	Mbps
CL-tRCD-tRP	5-5-5	5-5-5	4-4-4	3-3-3	CK

4.0 Absolute Maximum DC Rating

Symbol	Parameter	Rating	Units
V_{in} , Vout	Voltage on any pin relative to V_{SS}	-0.5 ~ 2.3	V
V_{DD}	Voltage on V_{DD} & V_{DDQ} supply relative to V_{ss}	-1.0 ~ 2.3	V
V_{DDQ}	Short circuit current	-0.5 ~ 2.3	V
V_{DDL}	Power dissipation	-0.5 ~ 2.3	V
T_{STG}	Storage Temperature	-55 ~ + 100	°C

5.0 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back	Pin	Back
1	VREF	51	DQS2	101	A1	151	DQ42	2	VSS	52	DM2	102	A0	152	DQ46
3	Vss	53	VSS	103	VDD	153	DQ43	4	DQ4	54	VSS	104	VDD	154	DQ47
5	DQ0	55	DQ18	105	A10/AP	155	VSS	6	DQ5	56	DQ22	106	BA1	156	VSS
7	DQ1	57	DQ19	107	BA0	157	DQ48	8	VSS	58	DQ23	108	RAS#	158	DQ52
9	VSS	59	VSS	109	WE#	159	DQ49	10	DM0	60	VSS	110	S0#	160	DQ53
11	DQS0#	61	DQ24	111	VDD	161	VSS	12	VSS	62	DQ28	112	VDD	162	VSS
13	DQS0	63	DQ25	113	CAS#	163	NC	14	DQ6	64	DQ29	114	ODT0	164	CK1
15	VSS	65	VSS	115	NC/S1#	165	VSS	16	DQ7	66	VSS	116	A13	166	CK1#
17	DQ2	67	DM3	117	VDD	167	DQS6#	18	VSS	68	DQS3#	118	VDD	168	VSS
19	DQ3	69	NC	119	ODT1	169	DQS6	20	DQ12	70	DQS3	120	NC	170	DM6
21	VSS	71	VSS	121	VSS	171	VSS	22	DQ13	72	VSS	122	VSS	172	VSS
23	DQ8	73	DQ26	123	DQ32	173	DQ50	24	VSS	74	DQ30	124	DQ36	174	DQ54
25	DQ9	75	DQ27	125	DQ33	175	DQ51	26	DM1	76	DQ31	126	DQ37	176	DQ55
27	VSS	77	VSS	127	VSS	177	VSS	28	VSS	78	VSS	128	VSS	178	VSS
29	DQS1#	79	CKE0	129	DQS4#	179	DQ56	30	CK0	80	CKE1	130	DM4	180	DQ60
31	DQS1	81	VDD	131	DQS4	181	DQ57	32	CK0#	82	VDD	132	VSS	182	DQ61
33	VSS	83	NC	133	VSS	183	VSS	34	VSS	84	NC	134	DQ38	184	VSS
35	DQ10	85	BA2	135	DQ34	185	DM7	36	DQ14	86	NC	136	DQ39	186	DQS7#
37	DQ11	87	VDD	137	DQ35	187	VSS	38	DQ15	88	VDD	138	VSS	188	DQS7
39	VSS	89	A12	139	VSS	189	DQ58	40	VSS	90	A11	140	DQ44	190	VSS
41	VSS	91	A9	141	DQ40	191	DQ59	42	VSS	92	A7	142	DQ45	192	DQ62
43	DQ16	93	A8	143	DQ41	193	VSS	44	DQ20	94	A6	144	VSS	194	DQ63
45	DQ17	95	VDD	145	VSS	195	SDA	46	DQ21	96	VDD	146	DQS5#	196	VSS
47	VSS	97	A5	147	DM5	197	SCL	48	VSS	98	A4	148	DQS5	198	SA0
49	DQS2#	99	A3	149	VSS	199	VDDSPD	50	NC	100	A2	150	VSS	200	SA1

6.0 Dimm Pin Description

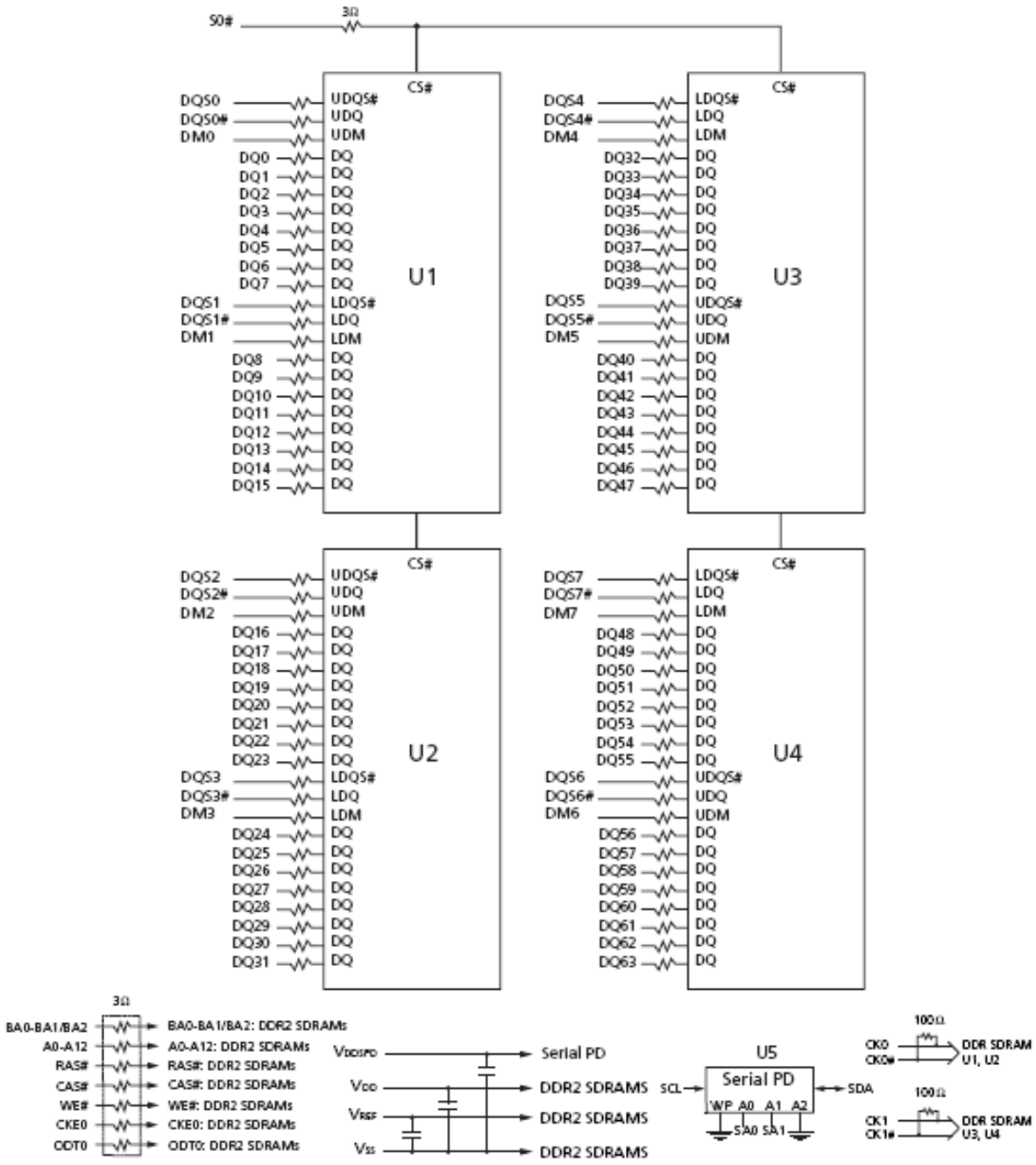
Pin Name	Function	Pin Name	Function
A0 ~ A9, A11 ~ A13	Address input (Multiplexed)	ODT0~ODT1	On Die Termination
A10/AP	Address Input/Autoprecharge	DQ0~DQ63	Data Input/Output
BA0 ~ BA1,BA2	Bank Select	CK0# ~ CK1#	Clock input, negative line
CK0 ~ CK1	Clock input	DM0 ~ DM7	Data Masks/Data strobes (Read)
CKE0, CKE1	Clock enable input	DQS0~DQS7	Data Strobes
S0#, S1#	Chip select input	DQS0#~DQS7#	Data strobes, negative line
RAS#	Row address strobe	V_{DD}	Core Power
CAS#	Column address strobe	V_{REF}	Input/Output Reference
WE#	Write Enable	V_{SS}	Ground
SCL	SPD Clock Input	V_{DDSPD}	SPD
SDA	SPD Data Input/Output	NC	No connection
SA0~SA1	SPD Address		

7.0 Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
32Mx8(256Mb) base	A0-A12	A0-A9	BA0-BA1	A10
64Mx8(512Mb) base	A0-A13	A0-A9	BA0-BA1	A10
32Mx16(512Mb) base	A0-A12	A0-A9	BA0-BA1	A10
64Mx16(1Gb) base	A0-A12	A0-A9	BA0-BA2	A10
128Mx8(1Gb) base	A0-A13	A0-A9	BA0-BA2	A10

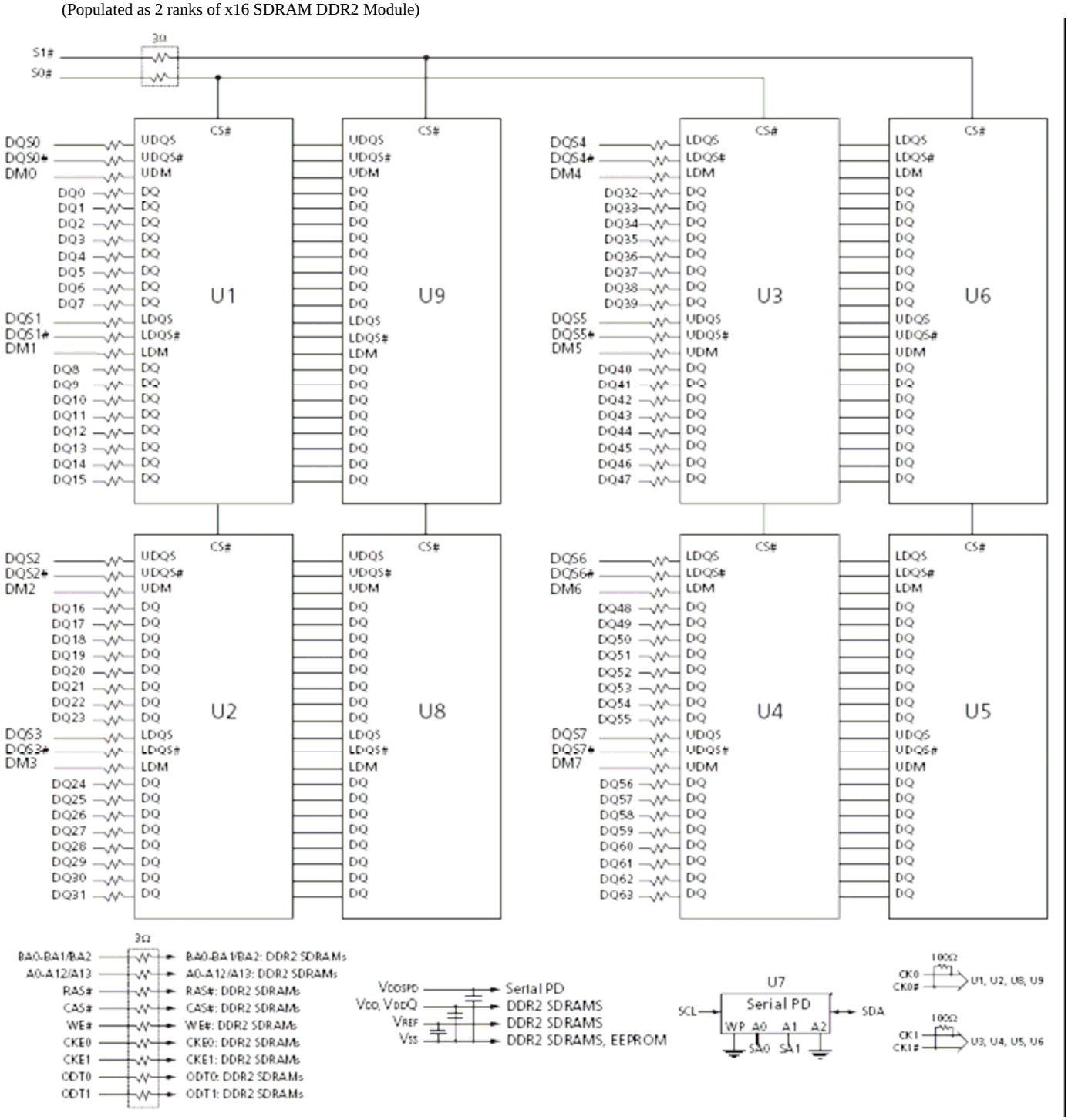
8.1 Functional Block Diagram: 256MB, 32Mx64 Module

(Populated as 1 rank of x16 SDRAM DDR2 Module)



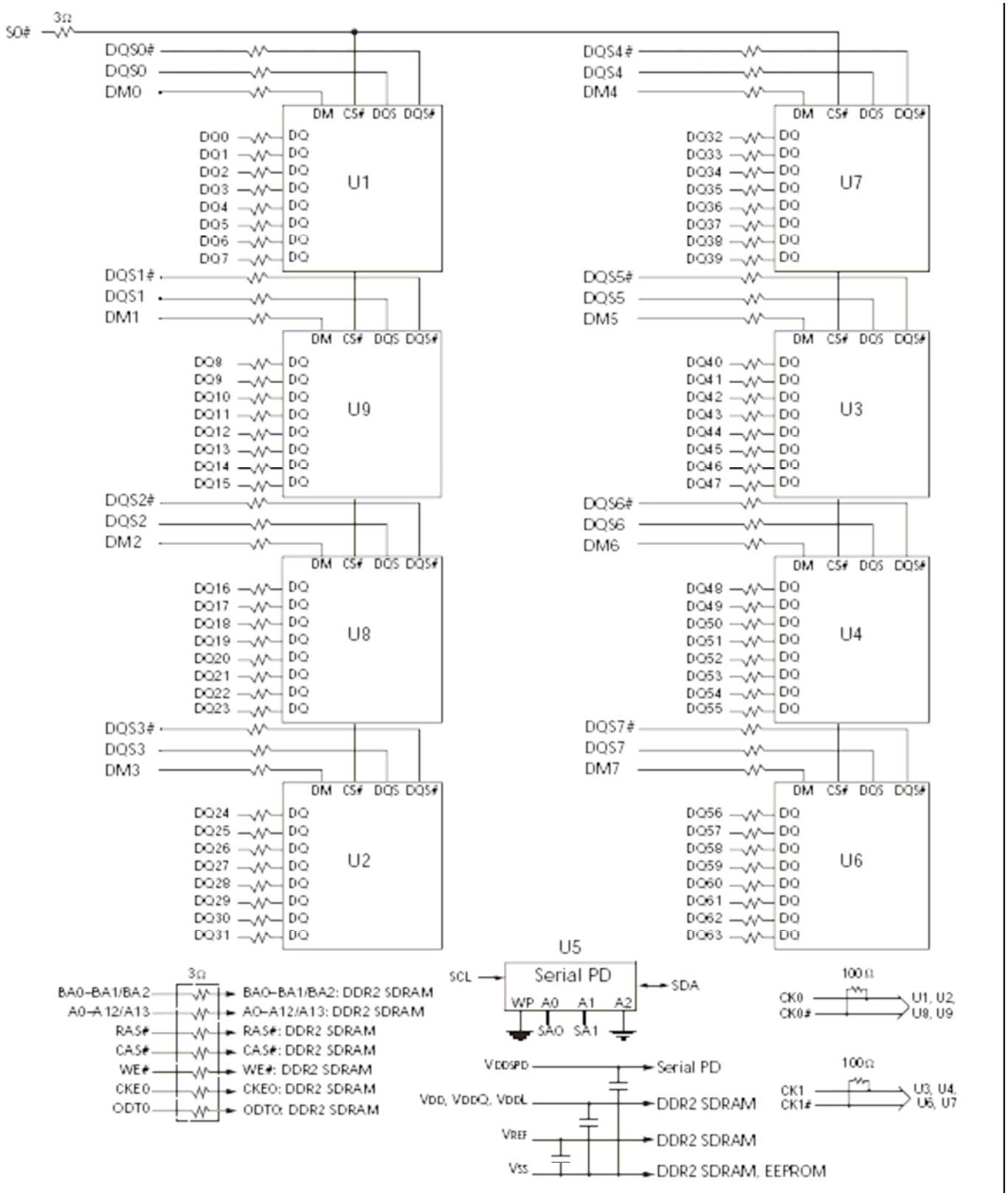
8.2 Functional Block Diagram: 512MB/1GB, 64Mx64/128Mx64 Module

(Populated as 2 ranks of x16 SDRAM DDR2 Module)



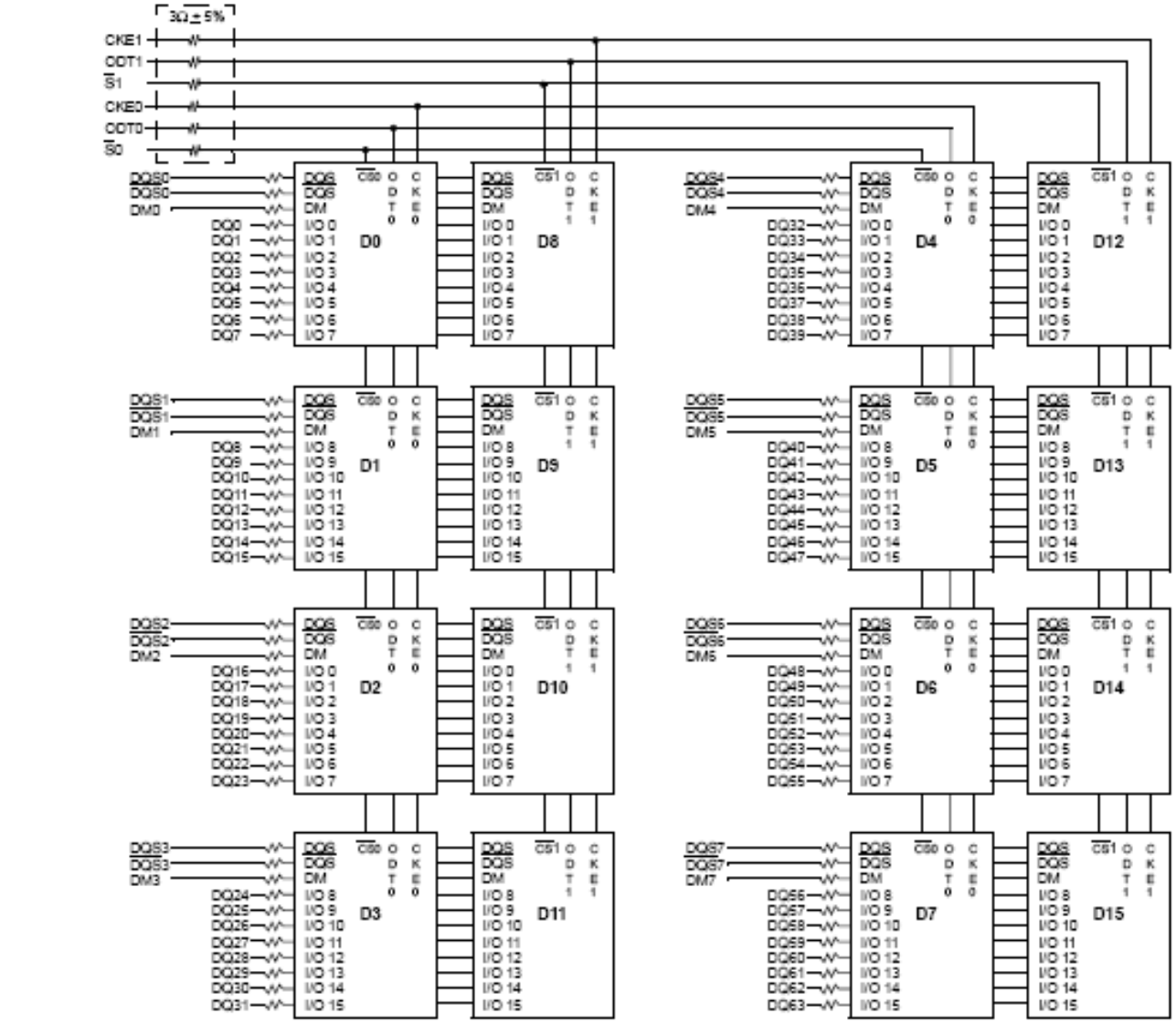
8.3 Functional Block Diagram: 256MB(32Mx64), 512MB(64Mx64), 1GB(128Mx64) Module

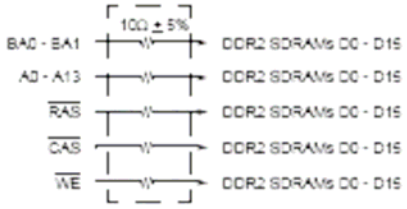
(Populated as 2 ranks of x8 SDRAM DDR2 Module)

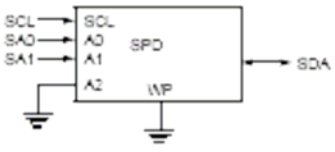


8.4 Functional Block Diagram: 1GB and 2GB, 128Mx64 and 256Mx64 Module

(Populated as 2 ranks of x8 SDRAM DDR2 Module)

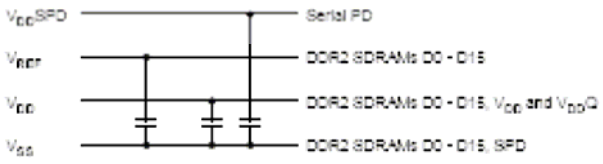






* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/CK0	8 DDR2 SDRAMs
*CK1/CK1	8 DDR2 SDRAMs

* Wire per Clock Loading Table/Wiring Diagrams



Notes :
1. DQ, DM, DQS/$\overline{DQS}$ resistors : 22 Ohms ± 5%.
2. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors : 10 Ohms ± 5%.

9.0 AC & DC Operating Conditions

Recommended operating conditions (Voltage referenced to Vss=0V, TA=0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	1.7	1.8	1.9	V
V_{DDL}	Supply Voltage for DLL	1.7	1.8	1.9	V
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V
V_{REF}	Input Reference Voltage	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	mV
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V

10.0 AC Timing Parameters & Specifications

(AC operating conditions unless otherwise noted)

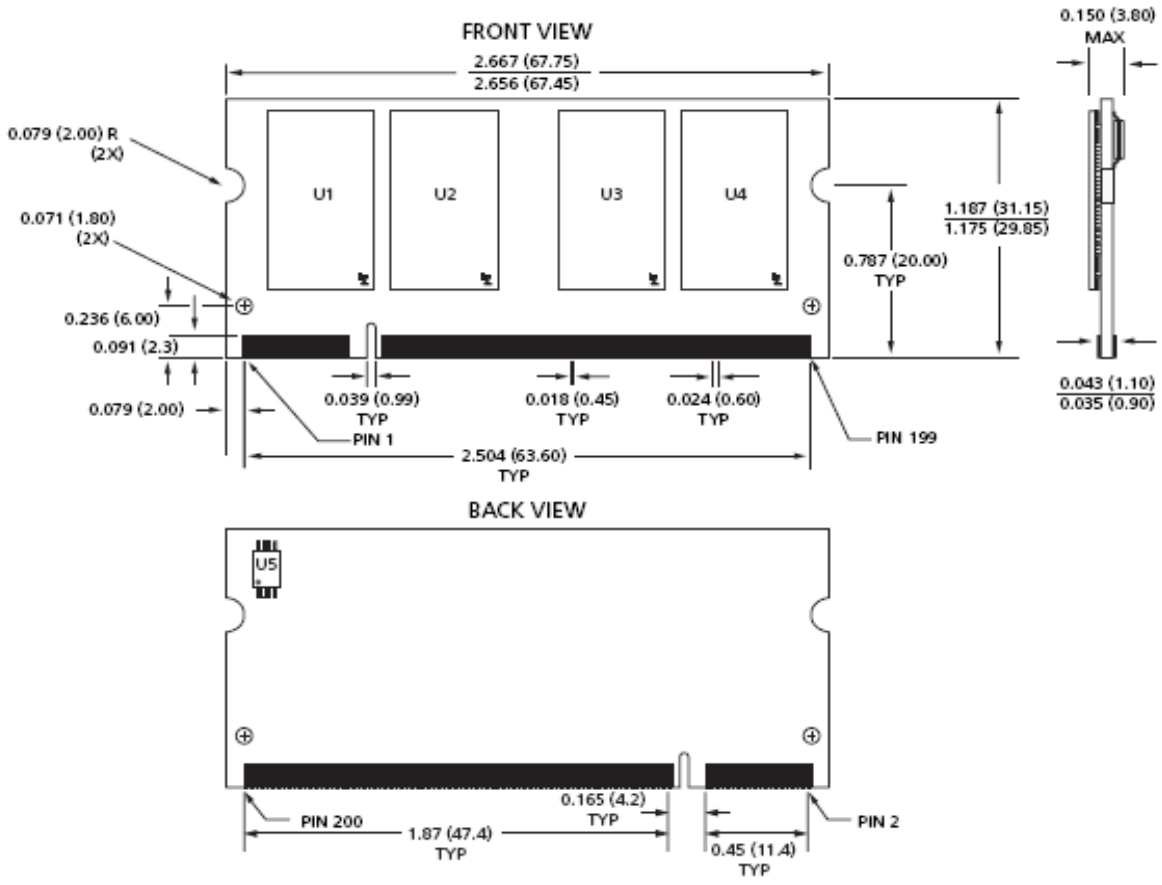
Parameter	Symbol	DDR2-800		DDR2-667		DDR2-533		DDR2-400		Units
		min	max	min	max	min	max	min	max	
DQ output access time from CK/$\overline{CK}$	tAC	- 400	+400	-450	+450	-500	+500	-600	+600	ps
DQS output access time from CK/$\overline{CK}$	tDQSCK	-350	+350	-400	+400	-450	+450	-500	+500	ps
CK high-level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
CK low-level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
CK half period	tHP	min(tCL ,tCH)	x	min(tCL, tCH	x	min(tCL, tCH	x	min(tCL, tCH	x	ps
Clock cycle time, CL=x	tCK	2500	8000	3000	8000	3750	8000	5000	8000	ps
DQ and DM input hold time	tDH(base)	125	x	175	x	225	x	275	x	ps
DQ and DM input setup time	tDS(base)	50	x	100	x	100	x	150	x	ps
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	0.6	x	0.6	x	tCK
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	0.35	x	0.35	x	tCK
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	x	tAC max	x	tAC max	x	tAC max	ps
DQS low-impedance time from CK/$\overline{CK}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	tAC min	tAC max	tAC min	tAC max	ps
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2*tAC min	tAC max	2*tAC min	tAC max	2*tAC min	tAC max	2*tAC min	tAC max	ps
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	200	x	240	x	300	x	350	ps
DQ hold skew factor	tQHS	x	300	x	340	x	400	x	450	ps
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	tHP - tQHS	x	tHP - tQHS	x	ps
First DQS latching transition to associated clock edge	tDQSS	-0.25	0.25	-0.25	0.25	-0.25	0.25	-0.25	0.25	tCK

Parameter	Symbol	DDR2-800		DDR2-667		DDR2-533		DDR2-400		Units
		min	max	min	max	min	max	min	max	
DQS input high pulse width	tDQSH	0.35	x	0.35	x	0.35	x	0.35	x	tCK
DQS input low pulse width	tDQSL	0.35	x	0.35	x	0.35	x	0.35	x	tCK
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	0.2	x	0.2	x	tCK
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	0.2	x	0.2	x	tCK
Mode register set command cycle timet	tMRD	2	x	2	x	2	x	2	x	tCK
Write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Write preamble	tWPRE	0.35	x	0.35	x	0.35	x	0.35	x	tCK
Address and control input hold time	tIH(base)	250	x	275	x	375	x	475	x	ps
Address and control input setup time	tIS(base)	175	x	200	x	250	x	350	x	ps
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Active to active command period for 1KB page size products	tRRD	7.5	x	7.5	x	7.5	x	7.5	x	ns
Active to active command period for 2KB page size products	tRRD	10	x	10	x	10	x	10	x	ns
Four Activate Window for 1KB page size productst	tFAW	35		37.5		37.5		37.5		ns
Four Activate Window for 2KB page size products	tFAW	45		50		50		50		ns
CAS to CAS command delay	tCCD	2	x	2		2		2		tCK
Write recovery time	tWR	15	x	15	x	15	x	15	x	ns
Auto precharge write recovery + precharge time	tDAL	WR+tRP	x	WR+ tRP	x	WR+tR P	x	WR+t RP	x	tCK
Internal write to read command delay	tWTR	7.5		7.5	x	7.5	x	10	x	ns
Internal read to precharge command delay	tRTP	7.5		7.5		7.5		7.5		ns
Exit self refresh to a non-read command	tXSNRt	tRFC + 10		tRFC + 10		tRFC + 10		tRFC + 10		ns
Exit self refresh to a read command	tXSRD	200		200		200		200		tCK
Exit precharge power down to any non-read command	tXP	2	x	2	x	2	x	2	x	tCK
Exit active power down to read command	tXARD	2	x	2	x	2	x	2	x	tCK
Exit active power down to read command(slow exit, lower power)	tXARDS	8 - AL		7 - AL		6 - AL		6 - AL		tCK
CKE minimum pulse width(high and low pulse width)	tCKE	3		3		3		3		tCK
ODT turn-on delay	tAOND	2	2	2	2	2	2	2	2	tCK
ODT turn-on	tAON	tAC(min)	tAC(max) + 0.7	tAC(min)	tAC(ma x)+0.7	tAC(mi n)	tAC(m ax)+1t	tAC(m in)	tAC(m ax)+1t	ns
ODT turn-on(Power-Down mode)	tAONPD	tAC(min) +2	2tCK +tAC(m ax)+1	tAC(min) +2	2tCK +tAC(m ax)+1	tAC(mi n)+2	2tCK +tAC(max)+ 1	tAC(m in)+2	2tCK +tAC(max)+ 1	ns
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	tCK
ODT turn-off	tAOF	tAC(min)	tAC(max)+ 0.6	tAC(min)	tAC(ma x)+ 0.6	tAC(mi n)	tAC(m ax)+ 0.6	tAC(m in)	tAC(m ax)+ 0.6	ns

Parameter	Symbol	DDR2-800		DDR2-667		DDR2-533		DDR2-400		Units
		min	max	min	max	min	max	min	max	
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5tCK+tAC(max)+1	tAC(min)+2	2.5tCK+tAC(max)+1	tAC(min)+2	2.5tCK+tAC(max)+1	tAC(min)+2	2.5tCK+tAC(max)+1	ns
ODT to power down entry latency	tANPD	3		3		3		3		tCK
ODT power down exit latency	tAXPD	8		8		8		8		tCK
OCD drive mode output delay	tOIT	0	12	0	12	0	12	0	12	ns
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		tIS+tCK+tIH		tIS+tCK+tIH		tIS+tCK+tIH		ns

11.1 Physical Dimensions: (32Mx16Based)
32Mx64 (1 Rank)

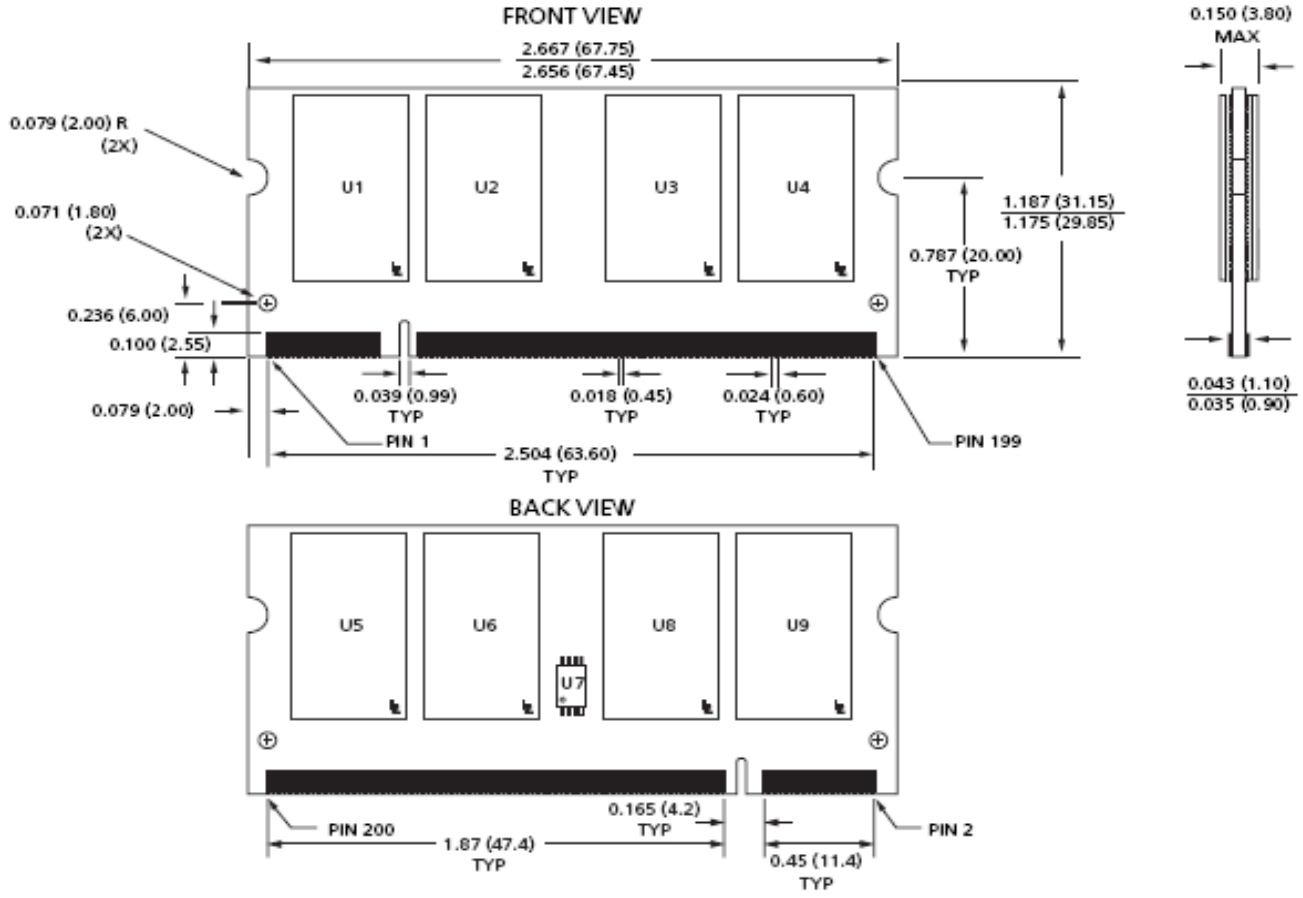
Units : Millimeters



Tolerances :± 0.005(.13) unless otherwise specified

11.2 Physical Dimensions: (32Mx8/64Mx8/128Mx8 Based) and (32Mx16/64Mx16 Based) 32Mx64/64Mx64/128Mx64 (1 Rank) and 64Mx64/128Mx64 (2 Ranks)

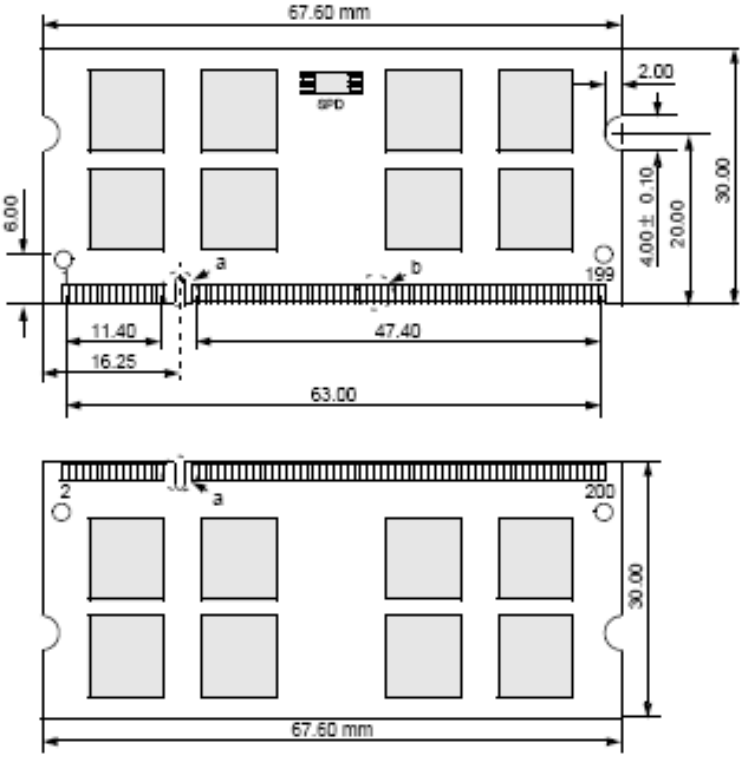
Units : Millimeters

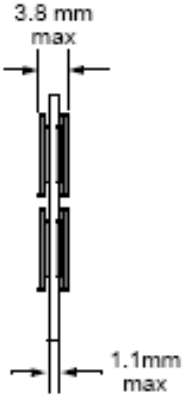


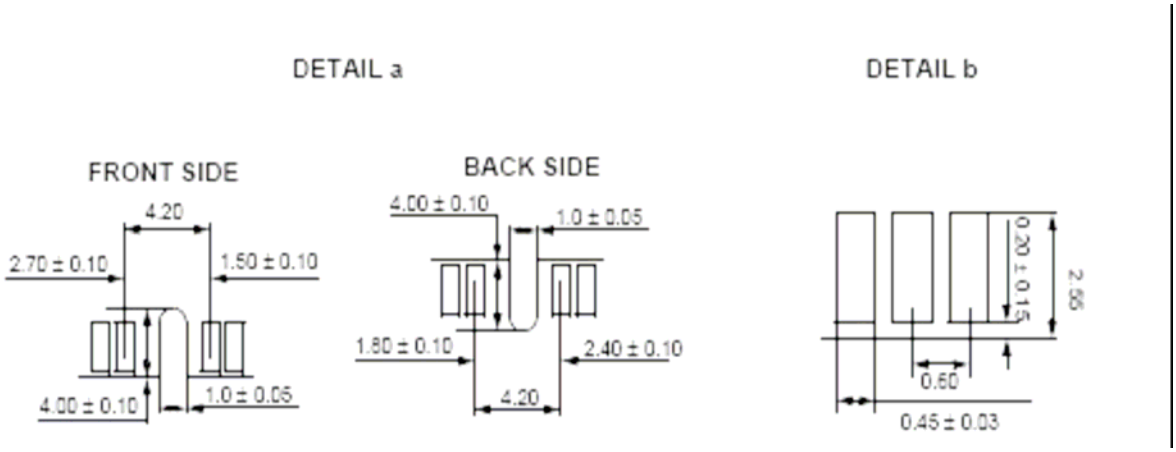
Tolerances :± 0.005(.13) unless otherwise specified

11.3 Physical Dimensions: (64Mx8/128Mx8 Based) 128Mx64/256Mx64 (2 Ranks)

Units : Millimeters







Tolerances :± 0.005(.13) unless otherwise specified