DDR2 Registered DIMM Module

256MB based on 256Mbit component

512MB, 1GB, 2GB based on 512Mbit component

60FBGA with Pb-Free

4GB based on 2Gbit and 2Gbit stack component

68FBGA with Pb-Free

Revision 1.0 (Mar. 2006)
-Initial Release

1.0 Feature

- JEDEC standard 1.8V +/- 0.1V Power Supply
- Standard Double-Data-Rate-Two Synchronous DRAMs with single 1.8V power supply
- Programmable CAS latencies (3,4,5,6), Burst Length (4 & 8) and Burst Type (Sequential / Interleave)
- Auto Refresh (CRB) and Self Refresh
- Bi-directional Differential Data Strobe (Single ended data strobe is option)
- Off Chip Driver (OCD) impedance adjustment
- On-Die termination with selectable values (50/75/150 ohms or disable)
- PASR (Partial Array Self Refresh)
- Average Refresh Period 7.8us at lower than a TCASE 85°C, 3.9us at 85°C < TCASE < 95 °C - support High Temperature Self-Refresh rate enable feature
- Serial presence detect with EEPROM
- RDIMM Dimension (Nominal) 30.00 mm high, 133.35 mm wide
- All speed grades faster than DDR400 comply with DDR400 timing specifications
- Based on JEDEC standard reference Raw Cards Lay out.
- RoHS compliant
- Gold plated contacts

2.0 Ordering Information

Part Number	Density	Config	Description / CL	DRAM Configuration/Components
	400 MHz	PC3200		
T400RA256	256MB	32M x 72	1 Bank, 3	32M x 8 (9 pcs)
T400RA512	512MB	64M x 72	1 Bank, 3	64M x 8 (9 pcs)
T400RA5124	512MB	64M x 72	1 Bank, 3	64M x 4 (18 pcs)
T400RA512I	512MB	64M x 72	1 Bank, 3	64M x 8 (9 pcs)
T400RA512M	512MB	64M x 72	1 Bank, 3	64M x 8 (9 pcs)
T400RB512	512MB	64M x 72	2 Bank, 3	32M x 8 (18 pcs)
T400RA1G4	1GB	128M x 72	1 Bank, 3	128M x 4 (18 pcs)
T400RB1G	1GB	128M x 72	2 Bank, 3	64M x 8 (18 pcs)
T400RB1GV	1GB	128M x 72	2 Bank, 3	64M x 8 (18 pcs)
T400RB1G_I	1GB	128M x 72	2 Bank, 3	64M x 8 (18 pcs)
T400RB1G_M	1GB	128M x 72	2 Bank, 3	64M x 8 (18 pcs)
T400RB2G4	2GB	256M x 72	2 Bank, 3	128M x 4 (36 pcs)
	533 MHz	PC4300		
T533RA256	256MB	32M x 72	1 Bank, 4	32M x 8 (9 pcs)
T533RA512	512MB	64M x 72	1 Bank, 4	64M x 8 (9 pcs)
T533RA5124	512MB	64M x 72	1 Bank, 4	64M x 4 (18 pcs)
T533RB512	512MB	64M x 72	2 Bank, 4	32M x 8 (18 pcs)
T533RA1G4	1GB	128M x 72	1 Bank, 4	128M x 4 (18 pcs)
T533RB1G	1GB	128M x 72	2 Bank, 4	64M x 8 (18 pcs)
T533RB2G4	2GB	256M x 72	2 Bank, 4	128M x 4 (36 pcs)
	667MHz	PC5300		
T667RA1G4	1GB	128M x 72	1 Bank, 5	128M x 4 (18 pcs)

T667RB1G	1GB	128M x 72	2 Bank, 5	64M x 8 (18 pcs)
T667RB2G4	2GB	256M x 72	2 Bank, 5	128M x 4 (36 pcs)
T667RA512	512MB	64M x 72	1 Bank, 5	64M x 8 (9 pcs)
	800MHz	**PC6400**		
T800RB1G	1GB	128M x 72	2 Bank, 5	64M x 8 (18 pcs)

3.0 Operating Frequencies

	DDR2-800	DDR2-667	DDR2-533	DDR-400	Unit
Speed @ CL3	400	400	400	400	Mbps
Speed @ CL4	533	533	533	400	Mbps
Speed @ CL5	800	667	-	-	Mbps
CL-tRCD-tRP	5-5-5	5-5-5	4-4-4	3-3-3	CK

4.0 Absolute Maximum DC Rating

Symbol	Parameter	Rating	Units
V_{in}, Vout	Voltage on any pin relative to V_{SS}	-0.5 ~ 2.3	V
V_{DD}	Voltage on V_{DD} & V_{DDQ} supply relative to V_{ss}	-1.0 ~ 2.3	V
V_{DDQ}	Short circuit current	-0.5 ~ 2.3	V
V_{DDL}	Power dissipation	-0.5 ~ 2.3	V
T_{STG}	Storage Temperature	-55 ~ + 100	°C

5.0 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	121	VSS	31	DQ19	151	VSS	61	A4	181	VDDQ	91	VSS	211	DM5/DQS14
2	VSS	122	DQ4	32	VSS	152	DQ28	62	VDDQ	182	A3	92	$\overline{DQS5}$	212	NC/$\overline{DQS14}$
3	DQ0	123	DQ5	33	DQ24	153	DQ29	63	A2	183	A1	93	DQS5	213	VSS
4	DQ1	124	VSS	34	DQ25	154	VSS	64	VDD	184	VDD	94	VSS	214	DQ46
5	VSS	125	DM0/DQS9	35	VSS	155	DM3/DQS12	KEY				95	DQ42	215	DQ47
6	$\overline{DQS0}$	126	NC/$\overline{DQS9}$	36	$\overline{DQS3}$	156	NC/$\overline{DQS12}$	65	VSS	185	CK0	96	DQ43	216	VSS
7	DQS0	127	VSS	37	DQS3	157	VSS	66	VSS	186	$\overline{CK0}$	97	VSS	217	DQ52
8	VSS	128	DQ6	38	VSS	158	DQ30	67	VDD	187	VDD	98	DQ48	218	DQ53
9	DQ2	129	DQ7	39	DQ26	159	DQ31	68	NC/Par_in	188	A0	99	DQ99	219	VSS
10	DQ3	130	VSS	40	DQ27	160	VSS	69	VDD	189	VDD	100	VSS	220	RFU
11	VSS	131	DQ12	41	VSS	161	CB4	70	A10/AP	190	BA1	101	SA2	221	RFU
12	DQ8	132	DQ13	42	CB0	162	CB5	71	BA0	191	VDDQ	102	NC(Test)	222	VSS
13	DQ9	133	VSS	43	CB1	163	VSS	72	VDDQ	192	$\overline{RAS}$	103	VSS	223	DM6/DQS15
14	VSS	134	DM1/DQS10	44	VSS	164	DM8/DQS17	73	$\overline{WE}$	193	S0	104	$\overline{DQS6}$	224	NC/$\overline{DQS15}$
15	$\overline{DQS1}$	135	NC/$\overline{DQS10}$	45	$\overline{DQS8}$	165	NC/$\overline{DQS17}$	74	$\overline{CAS}$	194	VDDQ	105	DQS6	225	VSS
16	DQS1	136	VSS	46	DQS8	166	VSS	75	VDDQ	195	ODT0	106	VSS	226	DQ54
17	VSS	137	RFU	47	VSS	167	CB6	76	S1	196	A13	107	DQ50	227	DQ55
18	$\overline{RESET}$	138	RFU	48	CB2	168	CB7	77	ODT1	197	VDD	108	DQ51	228	VSS
19	NC	139	VSS	49	CB3	169	VSS	78	VDDQ	198	VSS	109	VSS	229	DQ60
20	VSS	140	DQ14	50	VSS	170	VDDQ	79	VSS	199	DQ36	110	DQ56	230	DQ61
21	DQ10	141	DQ15	51	VDDQ	171	CKE1	80	DQ32	200	DQ37	111	DQ57	231	VSS
22	DQ11	142	VSS	52	CKE0	172	VDD	81	DQ33	201	VSS	112	VSS	232	DM7/DQS16
23	VSS	143	DQ20	53	VDD	173	NC	82	VSS	202	DM4/DQS13	113	$\overline{DQS7}$	233	NC/$\overline{DQS16}$
24	DQ16	144	DQ21	54	NC	174	NC	83	$\overline{DQS4}$	203	NC/$\overline{DQS13}$	114	DQS7	234	VSS
25	DQ17	145	VSS	55	NC/Err_Out	175	VDDQ	84	DQS4	204	VSS	115	VSS	235	DQ62
26	VSS	146	DM2/DQS11	56	VDDQ	176	A12	85	VSS	205	DQ38	116	DQ58	236	DQ63
27	$\overline{DQS2}$	147	NC/$\overline{DQS11}$	57	A11	177	A9	86	DQ34	206	DQ39	117	DQ59	237	VSS
28	DQS2	148	VSS	58	A7	178	VDD	87	DQ35	207	VSS	118	VSS	238	VDDSPD
29	VSS	149	DQ22	59	VDD	179	A8	88	VSS	208	DQ44	119	SDA	239	SA0
30	DQ18	150	DQ23	60	A5	180	A6	89	DQ40	209	DQ45	120	SCL	240	SA1
								90	DQ41	210	VSS				

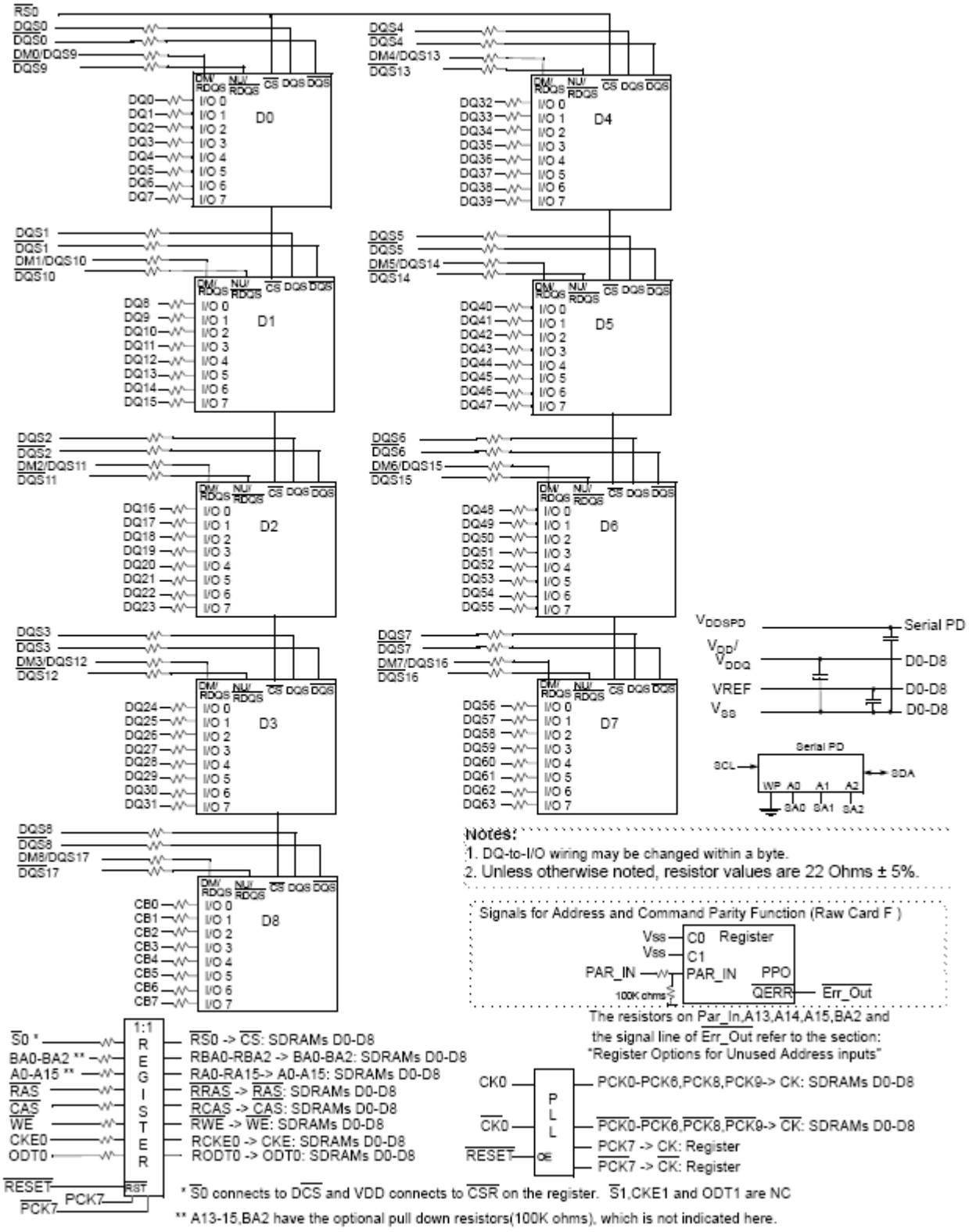
6.0 Dimm Pin Description

Pin Name	Function	Pin Name	Function
A0 ~ A9, A11~A14	Address input (Multiplexed)	ODT0~ODT1	On Die Termination
A10/AP	Address Input/Autoprecharge	CB0~CB7	Data check bits Input/Output
BA0 ~ BA2	Bank Select	DQ0~DQ63	Data Input/Output
CK0 ~ $\overline{CK0}$	Clock input, Clock input negative	$\overline{DQS0}$~$\overline{DQS8}$	Data strobes, negative line
CKE0, CKE1	Clock enable input	DM(0~8), DQS(9~17)	Data Masks/Data strobes (Read)
$\overline{S0}$, $\overline{S1}$	Chip select input	$\overline{DQS9}$~$\overline{DQS17}$	Data strobes (Read), negative line
$\overline{RAS}$	Row address strobe	DQS0~DQS8	Data Strobes
$\overline{CAS}$	Column address strobe	RFU	Reserved for future used
$\overline{WE}$	Write Enable	NC	No connection
SCL	SPD Clock Input	TEST	Memory bus test tool
SDA	SPD Data Input/Output	V_{DD}	Core Power
SA0~SA2	SPD Address	V_{DDQ}	I/O Power
Par_In	Parity bit for address & Control bus	V_{SS}	Ground
Err_Out	Parity error found in the Address and Control bus	V_{REF}	Input/Output Reference
Reset	Register and PLL control pin	V_{DDSPD}	SPD

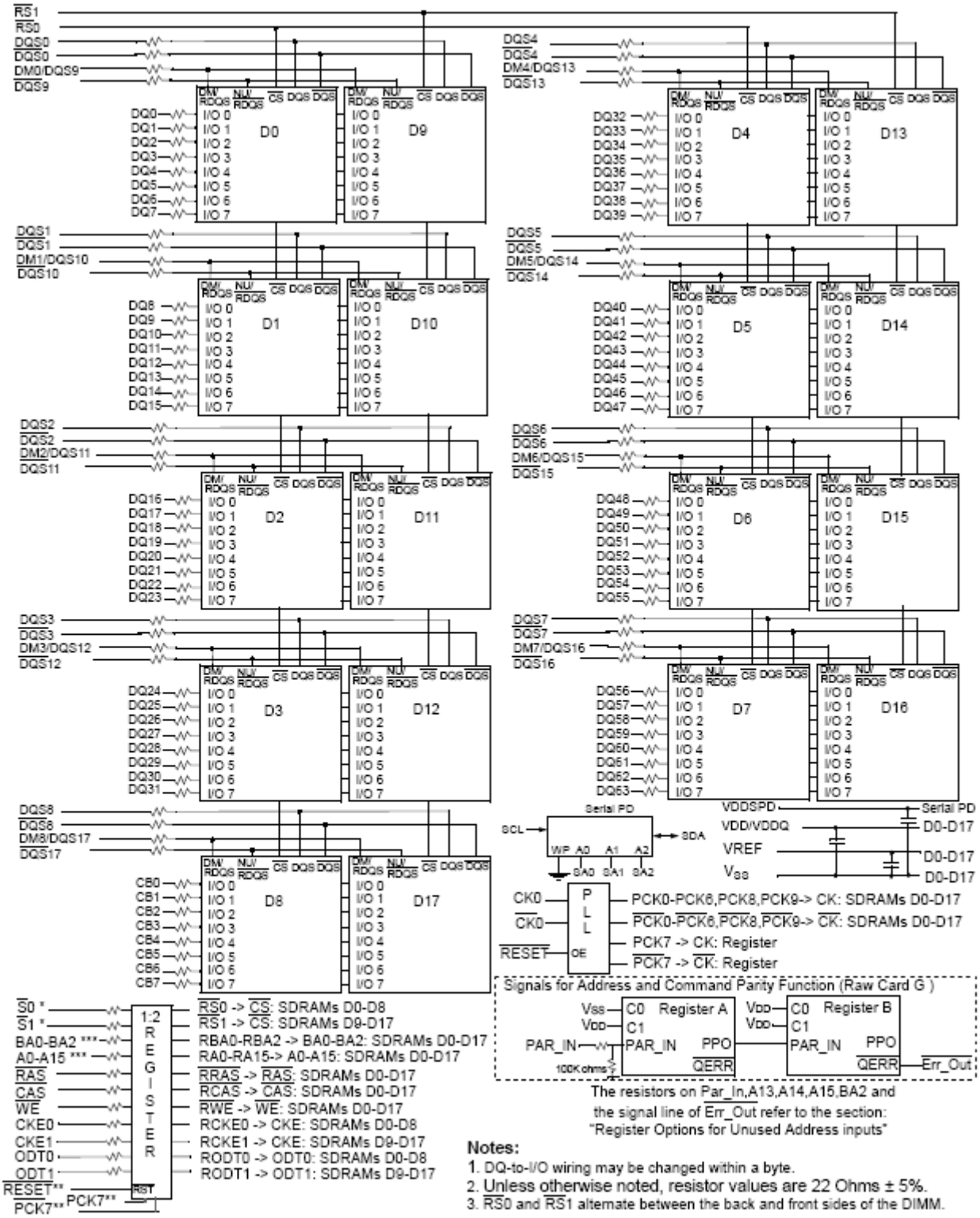
7.0 Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
128Mx4(512Mb) base	A0-A13	A0-A9, A11	BA0-BA1	A10
64Mx8(512Mb) base	A0-A13	A0-A9	BA0-BA1	A10
256Mx8(2Gb)base	A0-A14	A0-A9	BA0-BA2	A10
512Mx4(2Gb)base	A0-A14	A0-A9, A11	BA0-BA2	A10

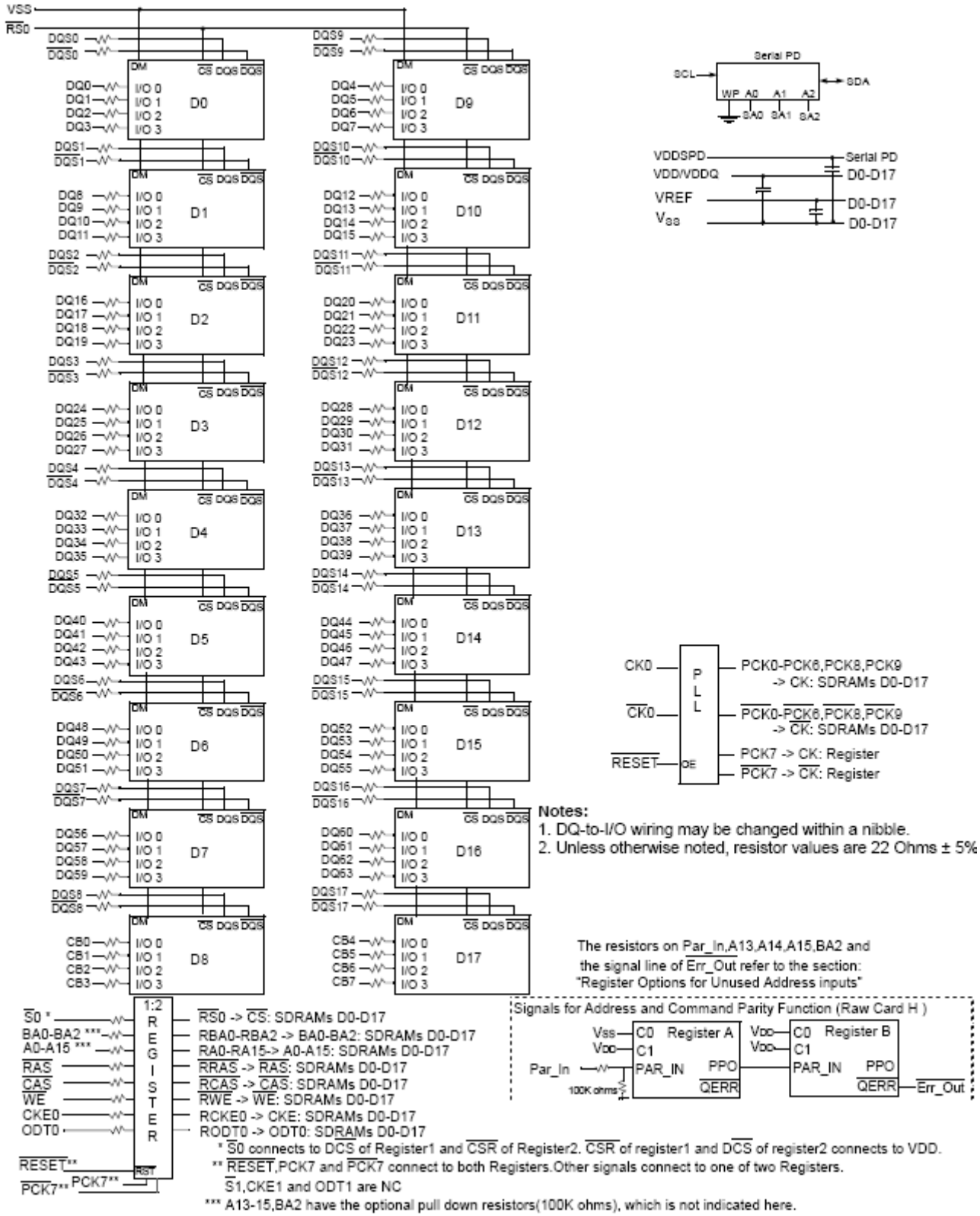
8.1 Functional Block Diagram: 512MB, 64x72 Module (Populated as 1 rank of x8 SDRAM Module)



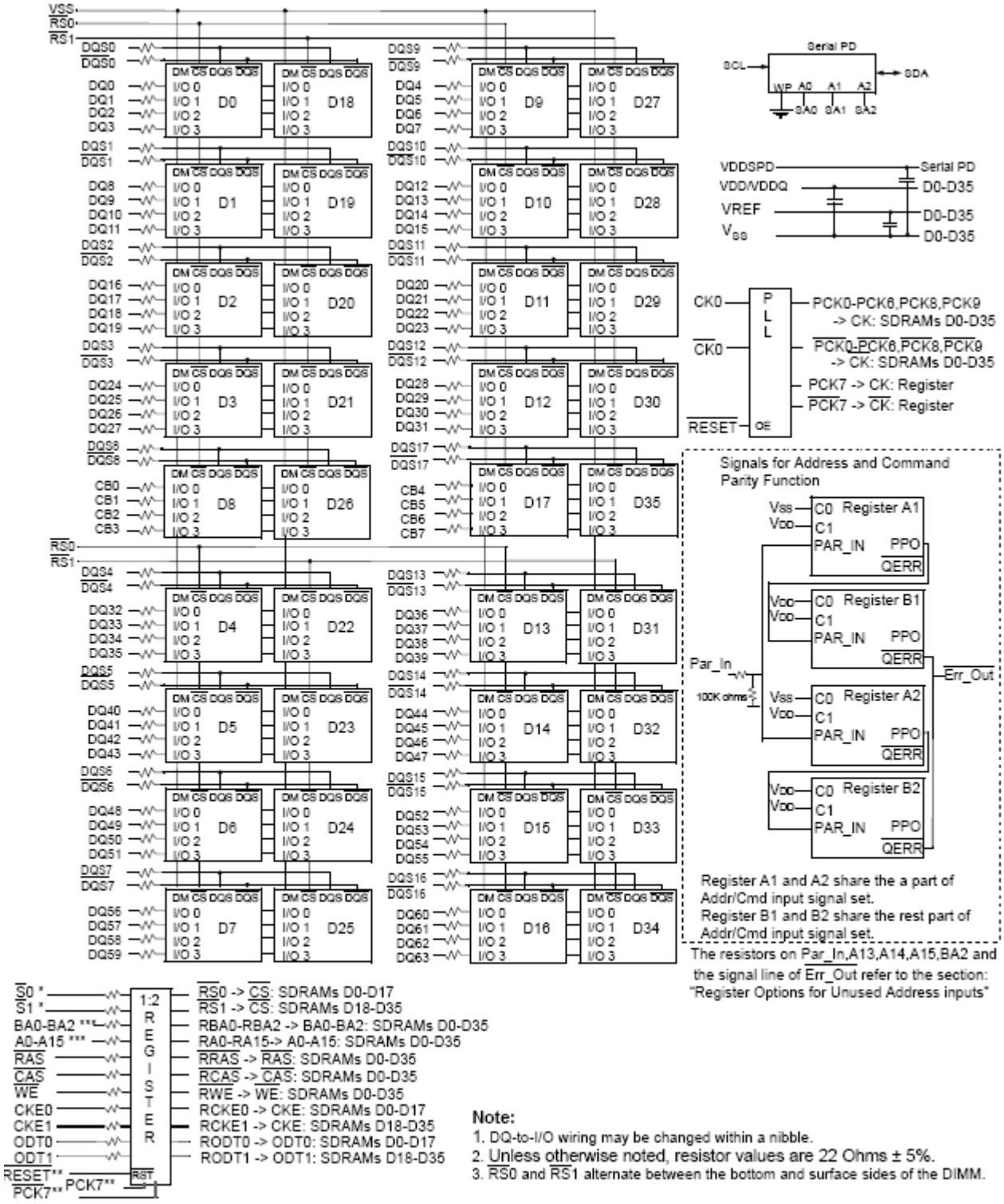
8.2 Functional Block Diagram: 1GB/ 4GB 128x72/512x72 Module (Populated as 2 ranks of x8 SDRAM Module)



8.3 Functional Block Diagram: 1GB, 128x72 Module (Populated as 1 rank of x4 SDRAM Module)



8.4 Functional Block Diagram: 2GB/4GB 256x72/512x72 Module (Populated as 2 ranks of x4 SDRAM Module)



9.0 AC & DC Operating Conditions

Recommended operating conditions (Voltage referenced to Vss=0V, TA=0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	1.7	1.8	1.9	V
V_{DDL}	Supply Voltage for DLL	1.7	1.8	1.9	V
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V
V_{REF}	Input Reference Voltage	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	mV
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V

10.0 Capacitance (Max.)

Symbol	Parameter/Condition	Min	Max	Unit
CCK	Input capacitance, CK and $\overline{CK}$	-	11	pF
CI1	Input capacitance, CKE and $\overline{CS}$	-	12	pF
CI2	Input capacitance, Addr, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	-	12	pF
CIO	Input capacitance, DQ, DM, DQS, $\overline{DQS}$	-	10	pF

11.0 AC Timing Parameters & Specifications

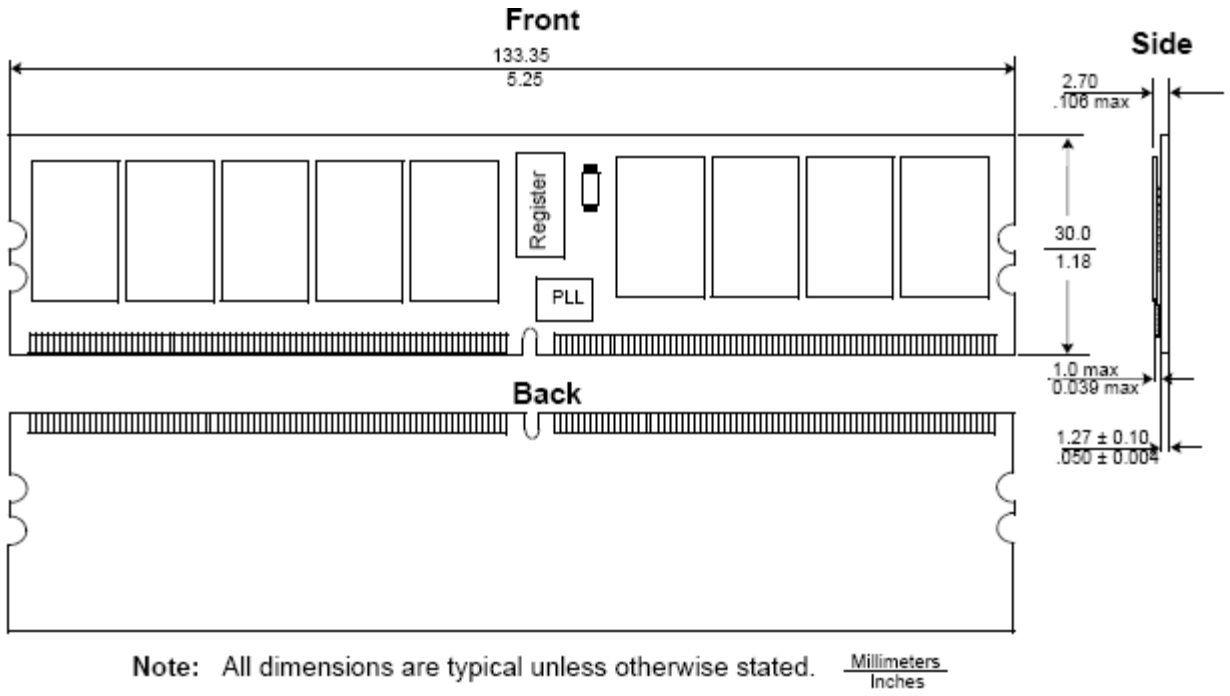
(AC operating conditions unless otherwise noted)

Parameter	Symbol	DDR2-800		DDR2-667		DDR2-533		DDR2-400		Units
		min	max	min	max	min	max	min	max	
DQ output access time from CK/$\overline{CK}$	tAC	- 400	+400	-450	+450	-500	+500	-600	+600	ps
DQS output access time from CK/$\overline{CK}$	tDQSCK	-350	+350	-400	+400	-450	+450	-500	+500	ps
CK high-level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
CK low-level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
CK half period	tHP	min(tCL ,tCH)	x	min(tCL, tCH	x	min(tCL, tCH	x	min(tCL, tCH	x	ps
Clock cycle time, CL=x	tCK	2500	8000	3000	8000	3750	8000	5000	8000	ps
DQ and DM input hold time	tDH(base)	125	x	175	x	225	x	275	x	ps
DQ and DM input setup time	tDS(base)	50	x	100	x	100	x	150	x	ps
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	0.6	x	0.6	x	tCK
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	0.35	x	0.35	x	tCK
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	x	tAC max	x	tAC max	x	tAC max	ps
DQS low-impedance time from CK/$\overline{CK}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	tAC min	tAC max	tAC min	tAC max	ps
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2*tAC min	tAC max	2*tAC min	tAC max	2*tAC min	tAC max	2*tAC min	tAC max	ps
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	200	x	240	x	300	x	350	ps
DQ hold skew factor	tQHS	x	300	x	340	x	400	x	450	ps
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	tHP - tQHS	x	tHP - tQHS	x	ps
First DQS latching transition to associated clock edge	tDQSS	-0.25	0.25	-0.25	0.25	-0.25	0.25	-0.25	0.25	tCK

Parameter	Symbol	DDR2-800		DDR2-667		DDR2-533		DDR2-400		Units
		min	max	min	max	min	max	min	max	
DQS input high pulse width	tDQSH	0.35	x	0.35	x	0.35	x	0.35	x	tCK
DQS input low pulse width	tDQSL	0.35	x	0.35	x	0.35	x	0.35	x	tCK
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	0.2	x	0.2	x	tCK
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	0.2	x	0.2	x	tCK
Mode register set command cycle timet	tMRD	2	x	2	x	2	x	2	x	tCK
Write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Write preamble	tWPRE	0.35	x	0.35	x	0.35	x	0.35	x	tCK
Address and control input hold time	tIH(base)	250	x	275	x	375	x	475	x	ps
Address and control input setup time	tIS(base)	175	x	200	x	250	x	350	x	ps
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Active to active command period for 1KB page size products	tRRD	7.5	x	7.5	x	7.5	x	7.5	x	ns
Active to active command period for 2KB page size products	tRRD	10	x	10	x	10	x	10	x	ns
Four Activate Window for 1KB page size productst	tFAW	35		37.5		37.5		37.5		ns
Four Activate Window for 2KB page size products	tFAW	45		50		50		50		ns
CAS to CAS command delay	tCCD	2	x	2		2		2		tCK
Write recovery time	tWR	15	x	15	x	15	x	15	x	ns
Auto precharge write recovery + precharge time	tDAL	WR+tRP	x	WR+ tRP	x	WR+tR P	x	WR+t RP	x	tCK
Internal write to read command delay	tWTR	7.5		7.5	x	7.5	x	10	x	ns
Internal read to precharge command delay	tRTP	7.5		7.5		7.5		7.5		ns
Exit self refresh to a non-read command	tXSNRt	tRFC + 10		tRFC + 10		tRFC + 10		tRFC + 10		ns
Exit self refresh to a read command	tXSRD	200		200		200		200		tCK
Exit precharge power down to any non-read command	tXP	2	x	2	x	2	x	2	x	tCK
Exit active power down to read command	tXARD	2	x	2	x	2	x	2	x	tCK
Exit active power down to read command(slow exit, lower power)	tXARDS	8 - AL		7 - AL		6 - AL		6 - AL		tCK
CKE minimum pulse width(high and low pulse width)	tCKE	3		3		3		3		tCK
ODT turn-on delay	tAOND	2	2	2	2	2	2	2	2	tCK
ODT turn-on	tAON	tAC(min)	tAC(max) + 0.7	tAC(min)	tAC(ma x)+0.7	tAC(mi n)	tAC(m ax)+1t	tAC(m in)	tAC(m ax)+1t	ns
ODT turn-on(Power-Down mode)	tAONPD	tAC(min) +2	2tCK +tAC(m ax)+1	tAC(min) +2	2tCK +tAC(m ax)+1	tAC(mi n)+2	2tCK +tAC(max)+ 1	tAC(m in)+2	2tCK +tAC(max)+ 1	ns
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	tCK
ODT turn-off	tAOF	tAC(min)	tAC(max)+ 0.6	tAC(min)	tAC(ma x)+ 0.6	tAC(mi n)	tAC(m ax)+ 0.6	tAC(m in)	tAC(m ax)+ 0.6	ns

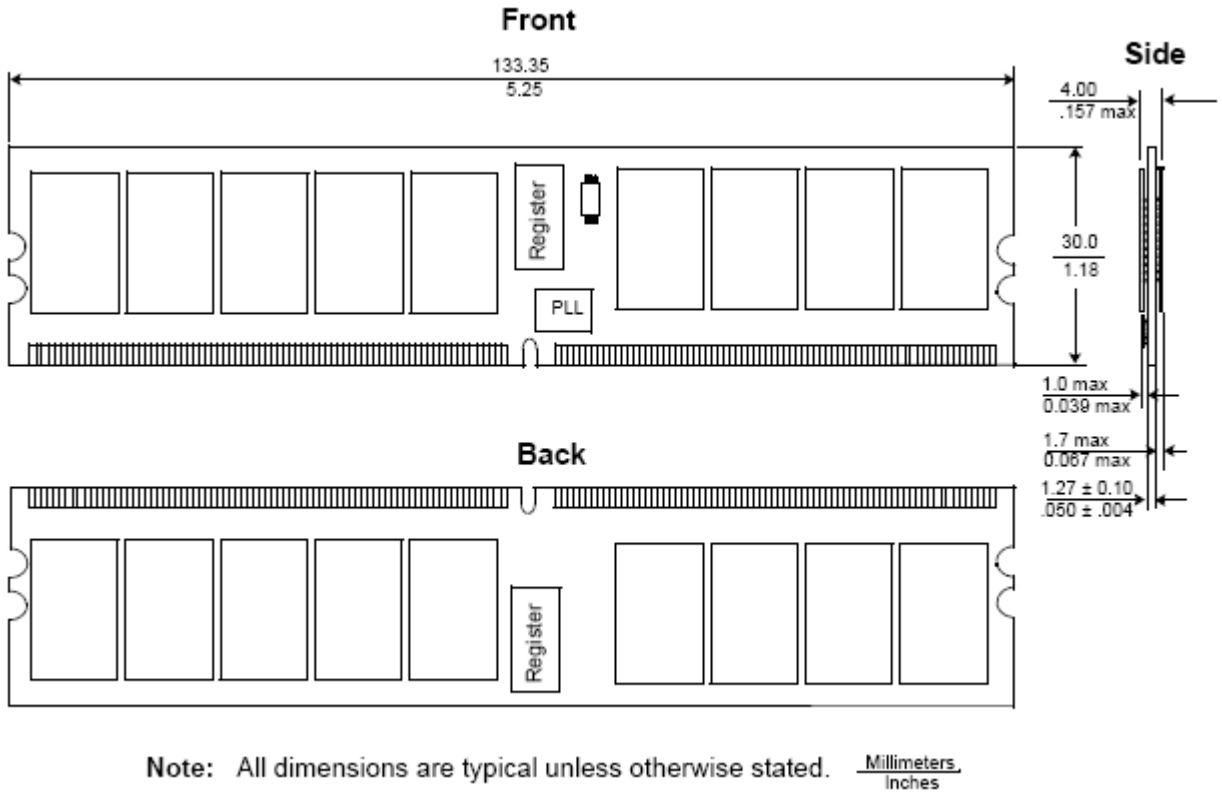
Parameter	Symbol	DDR2-800		DDR2-667		DDR2-533		DDR2-400		Units
		min	max	min	max	min	max	min	max	
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min) +2	2.5tCK +tAC(max)+1	tAC(min) +2	2.5tCK +tAC(max)+1	tAC(min)+2	2.5tCK +tAC(max)+1	tAC(min)+2	2.5tCK +tAC(max)+1	ns
ODT to power down entry latency	tANPD	3		3		3		3		tCK
ODT power down exit latency	tAXPD	8		8		8		8		tCK
OCD drive mode output delay	tOIT	0	12	0	12	0	12	0	12	ns
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK +tIH		tIS+tCK +tIH		tIS+tCK +tIH		tIS+tCK +tIH		ns

12.1 Physical Dimensions: (64Mx8Based)
64Mx72 (1 Rank)



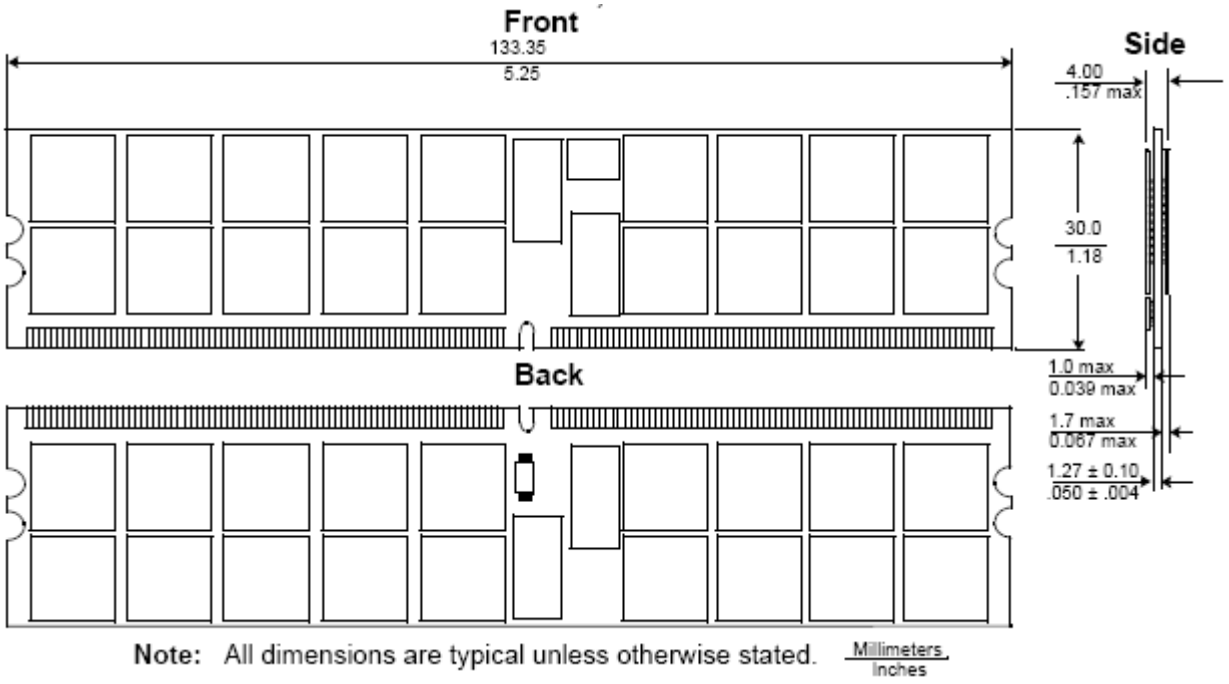
Note: All dimensions are typical unless otherwise stated. Millimeters / Inches

12.2 Physical Dimensions: (64Mx8/128Mbx4/256Mbx8 Based) 128Mx72/512Mx72 (1/2 Ranks)



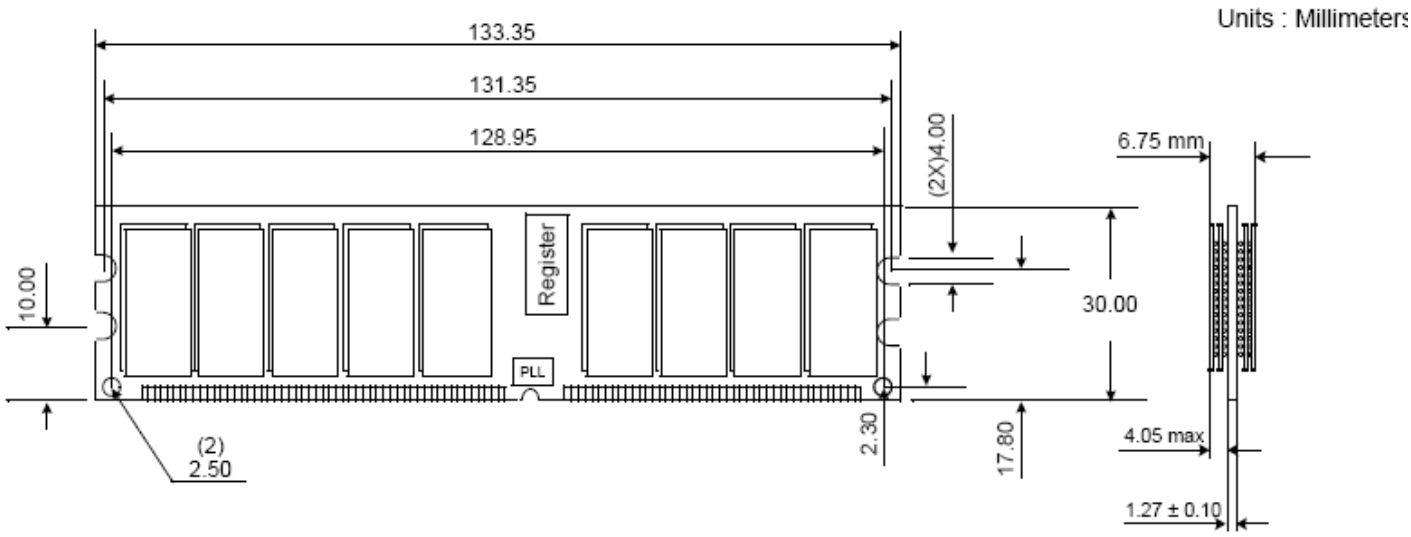
Tolerances :± 0.005(.13) unless otherwise specified

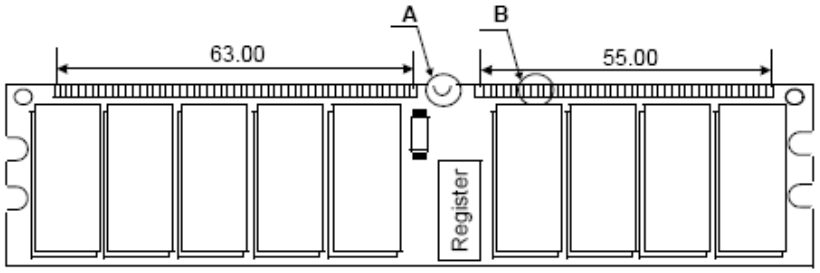
12.3 Physical Dimensions: (128Mx4Based)
256Mx72 (2 Ranks)

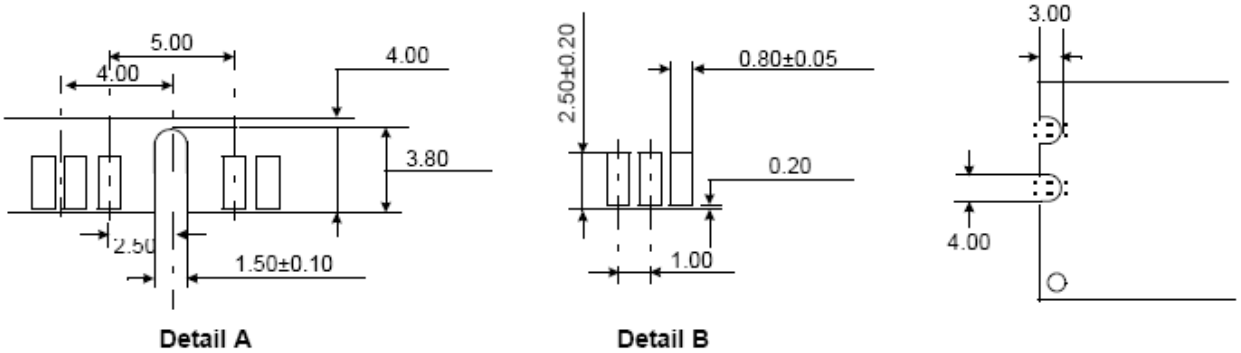


Tolerances :± 0.005(.13) unless otherwise specified

12.4 Physical Dimensions: (st.512Mbx4 based)
512Mx72 Module (2 Ranks)







Tolerances :± 0.005(.13) unless otherwise specified