

# **DDR4 SDRAM**

## **ECC-UnBuffered DIMM**

8GB based on 8Gbit (1Gx8) component



**Revision 1.0 (SEPT., 2015)**  
-Initial Release

**1. Features**

- Power Supply: VDD=1.2V (1.14V to 1.26V)
- VDDQ = 1.2V (1.14V to 1.26V)
- VPP - 2.5V (2.375V to 2.75V)
- VDDSPD=2.25V to 2.75V
- Functionality and operations comply with the DDR4 SDRAM datasheet
- 16 internal banks
- Bank Grouping is applied, and CAS to CAS latency (tCCD\_L, tCCD\_S) for the banks in the same or different bank group accesses are available
- Data transfer rates: PC4-2133, PC4-1866, PC4-1600
- Bi-Directional Differential Data Strobe
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
- Supports ECC error correction and detection
- On-Die Termination (ODT)
- Temperature sensor with integrated SPD
- This product is in compliance with the RoHS directive.
- Per DRAM Addressability is supported
- Internal Vref DQ level generation is available
- Write CRC is supported at all speed grades
- DBI (Data Bus Inversion) is supported(x8)
- CA parity (Command/Address Parity) mode is supported

**2. Ordering Information**

| Part Number | Density | Organization | Component Composition | # of Rank | Description |
|-------------|---------|--------------|-----------------------|-----------|-------------|
| F21EA8GS    | 8GB     | 1Gx72        | 1Gx8 x 9pcs           | 1         | PC4-17000   |

Note: Last character of the Part Number (x) represents DRAM vendor  
S=Samsung; M=Micron; H=Hynix

**3. Key Timing Parameters**

|             | DDR4-2133 | Unit |
|-------------|-----------|------|
| CL-tRCD-tRP | 15-15-15  | tCK  |
| CAS Latency | 14.06     | tCK  |
| tCK(min)    | 0.93      | ns   |
| tRCD(min)   | 14.06     | ns   |
| tRP(min)    | 14.06     | ns   |
| tRAS(min)   | 33        | ns   |
| tRC(min)    | 47.06     | ns   |

**4. Address Configuration**

| Organization   | Row Address | Column Address | Bank Address | Bank Group Address | Auto Pre-Charge |
|----------------|-------------|----------------|--------------|--------------------|-----------------|
| 1Gx8(8Gb) base | A0-A15      | A0-A9          | BA0-BA1      | BG0-BG1            | A10/AP          |

**5. DIMM Pin Descriptions**

The pin description table below is a comprehensive list of all possible pins for all DDR4 modules. Pins listed below may not be all supported on this module. Please see Pin Assignments for information specific to this module.

| Pin Name                            | Description   | Pin Name | Description   |
|-------------------------------------|---|----------|---|
| A0-A17 <sup>1</sup>                 | Register address input  | SCL      | I <sup>2</sup> C serial bus clock for SPD/TS and register     |
| BA0, BA1                            | Register bank select input                                    | SDA      | I <sup>2</sup> C serial data line for SPD/TS and register     |
| BG0, BG1                            | Register bank group select input                              | SA0-SA2  | I <sup>2</sup> C slave address select for SPD/TS and register |
| RAS_n <sup>2</sup>                  | Register row address strobe input                             | PAR      | Register parity input   |
| CAS_n <sup>3</sup>                  | Register column address strobe input                          | VDD      | SDRAM core power  |
| WE_n <sup>4</sup>                   | Register write enable input                                   |          |   |
| CS0_n, CS1_n, CS2_n, CS3_n          | DIMM Rank Select Lines input                                  | 12V      | Optional power supply on socket but not used on RDIMM         |
| CKE0, CEK1                          | Register clock enable lines input                             | VREFCA   | SDRAM command/address reference supply                        |
| ODT0, ODT1                          | Register on-die termination control lines input               | VSS      | Power supply return (ground)                                  |
| ACT_n                               | Register input for activate input                             | VDDSPD   | Serial SPD/TS positive power supply                           |
| DQ0-DQ63                            | DIMM memory data bus  | ALERT_n  | Register ALERT_n output                                       |
| CB0-CB7                             | DIMM ECC check bits   | VPP      | SDRAM Supply  |
| TDQS9_t-TDQS17_t<br>TDQS_c-TDQS17_c | Dummy loads for mixed populations of x4 based and x8          |          |   |
| DQS0_t-DQS17_t                      | Data Buffer data strobes (positive line of differential pair) | RESET_n  | Set Register and SDRAMs to a Known State                      |
| DBI0_n-DBI8_n                       | Data Bus Inversion  | EVENT_n  | SPD signals a thermal event has occurred                      |
| CK0_t, CK1_t                        | Register clock input (positive line of differential pair)     | VTT      | SDRAM I/O termination supply                                  |
| CK0_c, CK1_c                        | Register clock input (negative line of differential pair)     | RFU      | Reserved for future use                                       |

1. Address A17 is only valid for 16Gbx4 based SDRAMs.
2. RAS\_n is a multiplexed function with A16
3. CAS\_n is a multiplexed function with A15
4. WE\_n is a multiplexed function with A14

**6. Input/Output Functional Descriptions**

| Symbol        | Type  | Function  |
|---------------|-------|---|
| CK_t, CK_c    | Input | Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.   |
| CKE, (CKE1)   | Input | Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK_c, ODT, and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh. |
| CS_n, (CS1_n) | Input | Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.   |
| C0,C1,C2      | Input | Chip ID: Chip ID is only used for 3DS for 2, 4, 8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.  |

| Symbol  | Type              | Function  |
|---|-------------------|---|
| ODT, (ODT1)   | Input             | On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t,NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_c, DQSU_t, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.  |
| ACT_n   | Input             | Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14.  |
| RAS_n/A16,<br>CAS_n/A15,<br>WE_n/A14                        | Input             | Command Inputs RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multifunction. For example, for activation with ACT_n Low, those are Addressing like A16, A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table.   |
| DM_n/DBI_n/<br>TDQS_t,<br>(DMU_n/DBIU_n),<br>(DML_n/DBIL_n) | Input /<br>Output | Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8. |
| BG0 - BG1   | Input             | Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/8 have BG0 and BG1 but x16 has only BG0.   |
| BA0 - BA1   | Input             | Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.   |
| A0 - A17  | Input             | Address Inputs: Provided the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.   |
| A10 / AP  | Input             | Auto-precharge: A10 is sampled during Read/Write commands to determine whether Auto-precharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Auto-precharge; LOW: no Auto-precharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.  |
| A12 / BC_n  | Input             | Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.   |
| RESET_n   | Input             | Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V <sub>DD</sub> .   |

| Symbol                                       | Type          | Function  |
|--|---------------|---|
| DQ   | Input/ Output | Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific datasheets to determine which DQ is used.  |
| DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c | Input/ Output | Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t, and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended. |
| TDQS_t, TDQS_c                               | Output        | Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11, 12, 10 and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.           |
| PAR  | Input         | Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW.  |
| ALERT_n                                      | Output        | Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. IF there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until ongoing DRAM internal recovery transaction to complete.   |
| TEN  | Input         | Connectivity Test Mode Enable: Required on x16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this pin will enable boundary scan operation along with other pins. It is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.  |
| NC   |               | No Connect: No internal electrical connection is present.   |
| V <sub>DDQ</sub>                             | Supply        | DQ Power Supply: 1.2 V +/- 0.06 V   |
| V <sub>SSQ</sub>                             | Supply        | DQ Ground   |
| V <sub>DD</sub>                              | Supply        | Power Supply: 1.2 V +/- 0.06 V  |
| V <sub>SS</sub>                              | Supply        | Ground  |
| V <sub>PP</sub>                              | Supply        | DRAM Activation Power Supply: 2.5V (2.375V min , 2.75 max)  |
| V <sub>REFCA</sub>                           | Supply        | Reference voltage for CA  |
| ZQ   | Supply        | Reference Pin for ZQ calibration  |

**Note:** Input only pins (BG0-BG-1, BA0-BA1, A0-A17, ACT\_n, RAS\_n/A16, CAS\_n/A15, WE\_n/A14, CS\_n, CKE, ODT, and RESET\_n) do not supply termination.

**7. Pin Assignments**

| Pin | Front Side Pin Label                | Pin | Back Side Pin Label | Pin | Front Side Pin Label                | Pin | Back Side Pin Label |
|-----|-------------------------------------|-----|---------------------|-----|-------------------------------------|-----|---------------------|
| 1   | 12V, NC                             | 145 | 12V, NC             | 74  | CK0_t                               | 218 | CK1_t               |
| 2   | VSS                                 | 146 | VREFCA              | 75  | CK0_c                               | 219 | CK1_c               |
| 3   | DQ4                                 | 147 | VSS                 | 76  | VDD                                 | 220 | VDD                 |
| 4   | VSS                                 | 148 | DQ5                 | 77  | VTT                                 | 221 | VTT                 |
| 5   | DQ0                                 | 149 | VSS                 | KEY |                                     |     |                     |
| 6   | VSS                                 | 150 | DQ1                 |     |                                     |     |                     |
| 7   | TDQS9_t, DQS9_t,<br>DM0_n, DBI0_n   | 151 | VSS                 | 78  | EVENT_n                             | 222 | PARITY              |
| 8   | TDQS9_c, DQS9_c,<br>NC              | 152 | DQS0_c              | 79  | A0                                  | 223 | VDD                 |
| 9   | VSS                                 | 153 | DQS0_t              | 80  | VDD                                 | 224 | BA1                 |
| 10  | DQ6                                 | 154 | VSS                 | 81  | BA0                                 | 225 | A10/AP              |
| 11  | VSS                                 | 155 | DQ7                 | 82  | RAS_n/A16                           | 226 | VDD                 |
| 12  | DQ2                                 | 156 | VSS                 | 83  | VDD                                 | 227 | RFU                 |
| 13  | VSS                                 | 157 | DQ3                 | 84  | CS0_n                               | 228 | WE_n/A14            |
| 14  | DQ12                                | 158 | VSS                 | 85  | VDD                                 | 229 | VDD                 |
| 15  | VSS                                 | 159 | DQ13                | 86  | CAS_n/A15                           | 230 | NC, SAVE_n          |
| 16  | DQ8                                 | 160 | VSS                 | 87  | ODT0                                | 231 | VDD                 |
| 17  | VSS                                 | 161 | DQ9                 | 88  | VDD                                 | 232 | A13                 |
| 18  | TDQS10_t, DQS10_t,<br>DM1_n, DBI1_n | 162 | VSS                 | 89  | CS1_n, NC                           | 233 | VDD                 |
| 19  | TDQS10_c, DQS10_c,<br>NC            | 163 | DQS1_c              | 90  | VDD                                 | 234 | NC, A17             |
| 20  | VSS                                 | 164 | DQS1_t              | 91  | ODT1, NC                            | 235 | NC, C2              |
| 21  | DQ14                                | 165 | VSS                 | 92  | VDD                                 | 236 | VDD                 |
| 22  | VSS                                 | 166 | DQ15                | 93  | C0, CS2_n, NC                       | 237 | NC, CS3_n, C1       |
| 23  | DQ10                                | 167 | VSS                 | 94  | VSS                                 | 238 | SA2                 |
| 24  | VSS                                 | 168 | DQ11                | 95  | DQ36                                | 239 | VSS                 |
| 25  | DQ20                                | 169 | VSS                 | 96  | VSS                                 | 240 | DQ37                |
| 26  | VSS                                 | 170 | DQ21                | 97  | DQ32                                | 241 | VSS                 |
| 27  | DQ16                                | 171 | VSS                 | 98  | VSS                                 | 242 | DQ33                |
| 28  | VSS                                 | 172 | DQ17                | 99  | TDQS13_t, DQS13_t,<br>DM4_n, DBI4_n | 243 | VSS                 |
| 29  | TDQS11_t, DQS11_t,<br>DM2_n, DBI2_n | 173 | VSS                 | 100 | TDQS13_c, DQS13_c,<br>NC            | 244 | DQS4_c              |
| 30  | TDQS11_c, DQS11_c,<br>NC            | 174 | DQS2_c              | 101 | VSS                                 | 245 | DQS4_t              |
| 31  | VSS                                 | 175 | DQS2_t              | 102 | DQ38                                | 246 | VSS                 |
| 32  | DQ22                                | 176 | VSS                 | 103 | VSS                                 | 247 | DQ39                |
| 33  | VSS                                 | 177 | DQ23                | 104 | DQ34                                | 248 | VSS                 |
| 34  | DQ18                                | 178 | VSS                 | 105 | VSS                                 | 249 | DQ35                |

**Note:** Light colored text indicates functions that are not applicable for this design. An example is the NC for pin 56 because the products defined by this specification will always have DIMM wiring for this pin.

**288-pin ECC-UDIMM**

**DDR4 SDRAM**

| Pin | Front Side Pin Label                | Pin | Back Side Pin Label | Pin | Front Side Pin Label                | Pin | Back Side Pin Label |
|-----|-------------------------------------|-----|---------------------|-----|-------------------------------------|-----|---------------------|
| 35  | VSS                                 | 179 | DQ19                | 106 | DQ44                                | 250 | VSS                 |
| 36  | DQ28                                | 180 | VSS                 | 107 | VSS                                 | 251 | DQ45                |
| 37  | VSS                                 | 181 | DQ29                | 108 | DQ40                                | 252 | VSS                 |
| 38  | DQ24                                | 182 | VSS                 | 109 | VSS                                 | 253 | DQ41                |
| 39  | VSS                                 | 183 | DQ25                | 110 | TDQS14_t, DQS14_t,<br>DM5_n, DBI5_n | 254 | VSS                 |
| 40  | TDQS12_t, DQS12_t,<br>DM3_n, DBI3_n | 184 | VSS                 | 111 | TDQS14_c, DQS14_c,<br>NC            | 255 | DQS5_c              |
| 41  | TDQS12_c, DQS12_c,<br>NC            | 185 | DQS3_c              | 112 | VSS                                 | 256 | DQS3_t              |
| 42  | VSS                                 | 186 | DQS3_t              | 113 | DQ46                                | 257 | VSS                 |
| 43  | DQ30                                | 187 | VSS                 | 114 | VSS                                 | 258 | DQ47                |
| 44  | VSS                                 | 188 | DQ31                | 115 | DQ42                                | 259 | VSS                 |
| 45  | DQ26                                | 189 | VSS                 | 116 | VSS                                 | 260 | DQ43                |
| 46  | VSS                                 | 190 | DQ27                | 117 | DQ52                                | 261 | VSS                 |
| 47  | CB4, NC                             | 191 | VSS                 | 118 | VSS                                 | 262 | DQ53                |
| 48  | VSS                                 | 192 | CB5, NC             | 119 | DQ48                                | 263 | VSS                 |
| 49  | CB0, NC                             | 193 | VSS                 | 120 | VSS                                 | 264 | DQ49                |
| 50  | VSS                                 | 194 | CB1, NC             | 121 | TDQS15_t, DQS15_t,<br>DM6_n, DBI6_n | 265 | VSS                 |
| 51  | TDQS17_t, DQS17_t,<br>DM8_n, DBI8_n | 195 | VSS                 | 122 | TDQS15_c, DQS15_c,<br>NC            | 266 | DQS6_c              |
| 52  | TDQS17_c, DQS17_c,<br>NC            | 196 | DQS8_c              | 123 | VSS                                 | 267 | DQS6_t              |
| 53  | VSS                                 | 197 | DQS8_t              | 124 | DQ54                                | 268 | VSS                 |
| 54  | CB6, NC                             | 198 | VSS                 | 125 | VSS                                 | 269 | DQ55                |
| 55  | VSS                                 | 199 | CB7, NC             | 126 | DQ50                                | 270 | VSS                 |
| 56  | CB2, NC                             | 200 | VSS                 | 127 | VSS                                 | 271 | DQ51                |
| 57  | VSS                                 | 201 | CB3, NC             | 128 | DQ60                                | 272 | VSS                 |
| 58  | RESET_n                             | 202 | VSS                 | 129 | VSS                                 | 273 | DQ61                |
| 59  | VDD                                 | 203 | CKE1, NC            | 130 | DQ56                                | 274 | VSS                 |
| 60  | CKE0                                | 204 | VDD                 | 131 | VSS                                 | 275 | DQ57                |
| 61  | VDD                                 | 205 | RFU                 | 132 | TDQS16_t, DQS16_t,<br>DM7_n, DBI7_n | 276 | VSS                 |
| 62  | ACT_n                               | 206 | VDD                 | 133 | TDQS15_t, DQS_c,<br>NC              | 277 | DQS7_c              |
| 63  | BG0                                 | 207 | BG1                 | 134 | VSS                                 | 278 | DQS7_t              |
| 64  | VDD                                 | 208 | ALERT_n             | 135 | DQ62                                | 279 | VSS                 |
| 65  | A12/BC_n                            | 209 | VDD                 | 136 | VSS                                 | 280 | DQ63                |
| 66  | A9                                  | 210 | A11                 | 137 | DQ58                                | 281 | VSS                 |
| 67  | VDD                                 | 211 | A7                  | 138 | VSS                                 | 282 | DQ59                |
| 68  | A8                                  | 213 | A5                  | 139 | SA0                                 | 283 | VSS                 |

**Note:** Light colored text indicates functions that are not applicable for this design. An example is the NC for pin 56 because the products defined by this specification will always have DIMM wiring for this pin.

## 288-pin ECC-UDIMM

## DDR4 SDRAM

| Pin | Front Side Pin Label | Pin | Back Side Pin Label | Pin | Front Side Pin Label | Pin | Back Side Pin Label |
|-----|----------------------|-----|---------------------|-----|----------------------|-----|---------------------|
| 69  | A6                   | 214 | A4                  | 140 | SA1                  | 284 | VDDSPD              |
| 70  | VDD                  | 215 | VDD                 | 141 | SCL                  | 285 | SDA                 |
| 71  | A3                   | 215 | VDD                 | 142 | VPP                  | 286 | VPP                 |
| 72  | A1                   | 216 | A2                  | 143 | VPP                  | 287 | VPP                 |
| 73  | VDD                  | 217 | VDD                 | 144 | RFU                  | 288 | VPP                 |

**Note:** Light colored text indicates functions that are not applicable for this design. An example is the NC for pin 56 because the products defined by this specification will always have DIMM wiring for this pin.

### 8. Absolute Maximum DC Ratings

| Symbol                             | Parameter                           | Rating      | Units | NOTE |
|------------------------------------|-------------------------------------|-------------|-------|------|
| VDD                                | Voltage on VDD pin relative to Vss  | -0.3 ~ 1.5  | V     | 1,3  |
| VDDQ                               | Voltage on VDDQ pin relative to Vss | -0.3 ~ 1.5  | V     | 1,3  |
| VPP                                | Voltage on VPP pin relative to Vss  | -0.3 ~ 3.0  | V     | 4    |
| V <sub>IN</sub> , V <sub>OUT</sub> | Voltage on any pin relative to Vss  | -0.3 ~ 1.5  | V     | 1    |
| T <sub>STG</sub>                   | Storage Temperature                 | -55 to +100 | °C    | 1,2  |

**Note:**

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- VDD and VDDQ must be within 300 mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ. When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV
- VPP must be equal or greater than VDD/VDDQ at all times

### 9. DRAM Component Operating Temperature Range

| Symbol            | Parameter                          | Rating   | Units | NOTE |
|-------------------|------------------------------------|----------|-------|------|
| T <sub>OPER</sub> | Normal Operating Temperature Range | 0 to 85  | °C    | 1,2  |
|                   | Extended Temperature Range         | 85 to 95 | °C    | 1,3  |

**Note:**

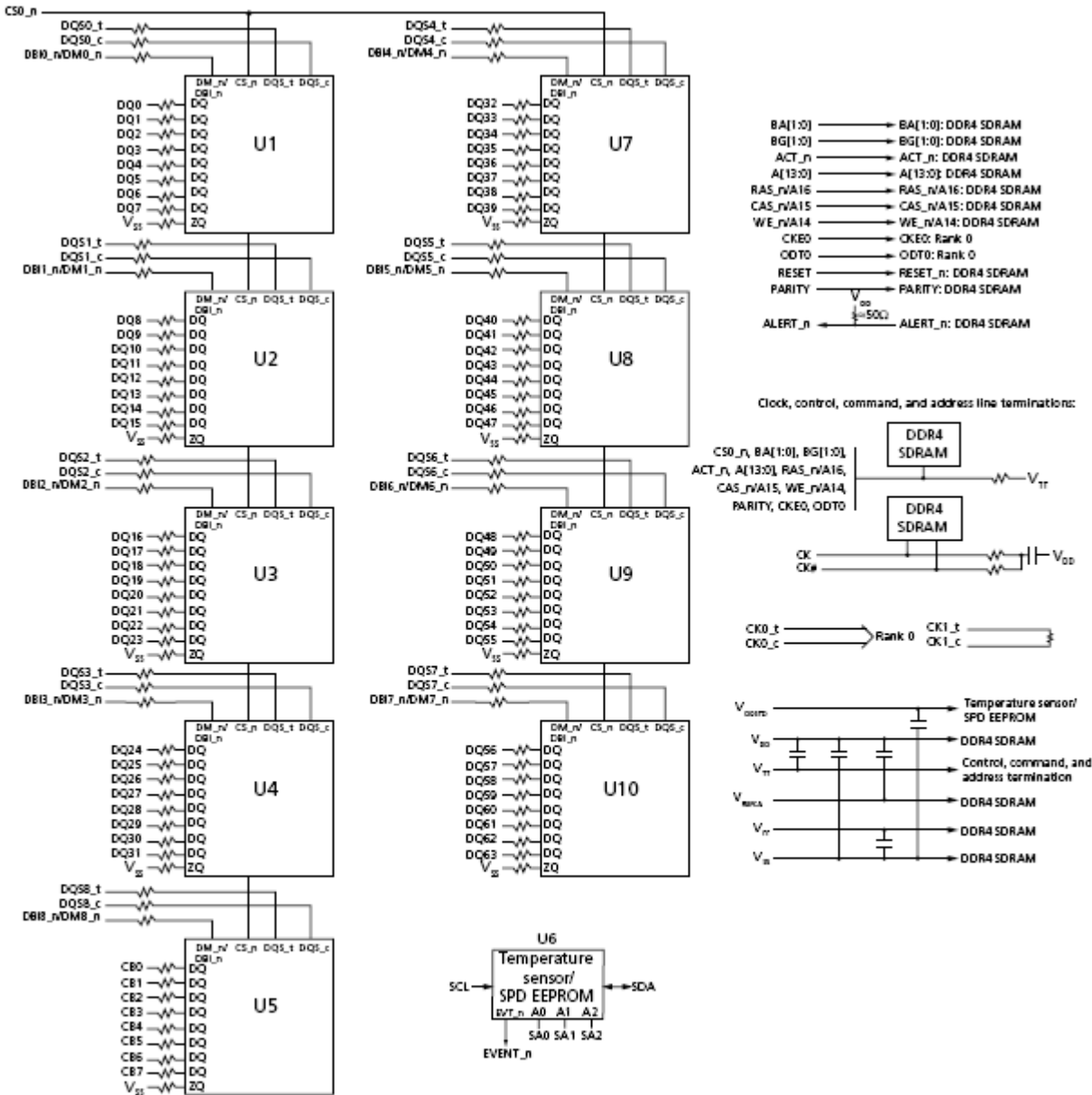
- Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85°C under all operating conditions.
- Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
  - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability
  - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). DDR4 SDRAMs support Auto Self-Refresh and in Extended Temperature Range and please refer to component datasheet and/or the DIMM SPD for tREFI requirements in the Extended Temperature Range



**288-pin ECC-UDIMM**

**DDR4 SDRAM**

**10. Functional Block Diagram: 8GB; 1Gx72 Module (1R x8)**



Note: 1. The ZQ ball on each DDR4 component is connected to an external  $240\Omega \pm 1\%$  resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

**NOTE:**

1. Unless otherwise noted, resistor values are  $15\Omega \pm 5\%$
2. See the net structure diagrams for resistors associated with the command, address and control bus.
3. ZQ resistors are  $240\Omega \pm 1\%$ . For all other resistor values refer to the appropriate wiring diagram.

**11.AC&DC Operating Conditions**

Recommended operating conditions (Voltage referred to Vss=0V, TA=0 to 70°C)

| Symbol           | Parameter                 | Min   | Typ | Max  | Unit |
|------------------|---------------------------|-------|-----|------|------|
| V <sub>DD</sub>  | Supply Voltage            | 1.14  | 1.2 | 1.26 | V    |
| V <sub>DDQ</sub> | Supply Voltage for Output | 1.14  | 1.2 | 1.26 | V    |
| V <sub>PP</sub>  |                           | 2.375 | 2.5 | 2.75 | V    |

**12.Input/Output Capacitance**

| Symbol                  | Parameter  | DDR4-2133 |      | DDR4-2400 |      | Unit | NOTE     |
|-------------------------|--|-----------|------|-----------|------|------|----------|
|                         |  | min       | max  | min       | max  |      |          |
| C <sub>IO</sub>         | Input/output capacitance   | 0.7       | 1.4  | 0.7       | 1.3  | p    | 1,2,3    |
| C <sub>DIO</sub>        | Input/output capacitance delta                                       | -0.1      | 0.1  | -0.1      | 0.1  | p    | 1,2,3,11 |
| C <sub>DDQS</sub>       | Input/output capacitance delta DQS <sub>t</sub> and DQS <sub>c</sub> | -         | 0.05 | -         | 0.05 | p    | 1,2,3,5  |
| C <sub>CK</sub>         | Input capacitance, CK <sub>t</sub> and CK <sub>c</sub>               | 0.2       | 0.8  | 0.2       | 0.7  | p    | 1,3      |
| C <sub>DCK</sub>        | Input capacitance delta CK <sub>t</sub> and CK <sub>c</sub>          | -         | 0.05 | -         | 0.05 | p    | 1,3,4    |
| C <sub>I</sub>          | Input capacitance(CTRL, ADD, CMD pins only)                          | 0.2       | 0.8  | 0.2       | 0.7  | p    | 1,3,6    |
| C <sub>DI_CTRL</sub>    | Input capacitance delta(All CTRL pins only)                          | -0.1      | 0.1  | -0.1      | 0.1  | p    | 1,3,7,8  |
| C <sub>DI_ADD_CMD</sub> | Input capacitance delta(All ADD/CMD pins only)                       | -0.1      | 0.1  | -0.1      | 0.1  | p    | 1,2,9,10 |
| C <sub>ALERT</sub>      | Input/output capacitance of ALERT                                    | 0.5       | 1.5  | 0.5       | 1.5  | p    | 1,3      |
| C <sub>ZQ</sub>         | Input/output capacitance of ZQ                                       | 0.5       | 2.3  | 0.5       | 2.3  | p    | 1,3,12   |
| C <sub>TEN</sub>        | Input capacitance of TEN   | 0.2       | 2.3  | 0.2       | 2.3  | p    | 1,3,13   |

**Note:**

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure TBD.
2. DQ, DM<sub>n</sub>, DQS<sub>T</sub>, DQS<sub>c</sub>, TDQS<sub>T</sub>, TDQS<sub>C</sub>. Although the DM, TDQS<sub>T</sub> and TDQS<sub>C</sub> pins have different functions, the loading matches DQ and DQS
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value CK<sub>T</sub>-CK<sub>C</sub>
5. Absolute value of CIO(DQS<sub>T</sub>)-CIO(DQS<sub>c</sub>)
6. CI applies to ODT, CS<sub>n</sub>, CKE, A0-A17, BA0-BA1, BG0-BG1, RAS<sub>n</sub>/A16, CAS<sub>n</sub>/A15, WE<sub>n</sub>/A14, ACT<sub>n</sub> and PAR.
7. CDI CTRL applies to ODT, CS<sub>n</sub> and CKE
8. CDI\_CTRL = CI(CTRL)-0.5\*(CI(CLK<sub>T</sub>)+CI(CLK<sub>C</sub>))
9. CDI\_ADD\_CMD applies to, A0-A17, BA0-BA1, BG0-BG1,RAS<sub>n</sub>/A16, CAS<sub>n</sub>/A15, WE<sub>n</sub>/A14, ACT<sub>n</sub> and PAR.
10. CDI\_ADD\_CMD = CI(ADD\_CMD)-0.5\*(CI(CLK<sub>T</sub>)+CI(CLK<sub>C</sub>))
11. CDIO = CIO(DQ,DM)-0.5\*(CIO(DQS<sub>T</sub>)+CIO(DQS<sub>c</sub>))
12. Maximum external load capacitance on ZQ pin: tbd pF.
13. TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.

**13.AC Timing Parameters & Specifications**  
(AC operating conditions unless otherwise noted)

| Speed   |                | DDR4-1866  |                                  | DDR4-2133                       |                                  | DDR4-2400                       |                                  | Units    | NOTE  |
|---|----------------|--|----------------------------------|---------------------------------|----------------------------------|---------------------------------|----------------------------------|----------|-------|
| Parameter   | Symbol         | MIN  | MAX                              | MIN                             | MAX                              | MIN                             | MAX                              |          |       |
| <b>Clock Timing</b>   |                |  |                                  |                                 |                                  |                                 |                                  |          |       |
| Minimum Clock Cycle Time (DLL off mode)   | tCK (DLL_OFF)  | 8  | -                                | 8                               | -                                | 8                               | -                                | ns       | 22    |
| Average Clock Period  | tCK(avg)       | 1.071  | <1.25                            | 0.938                           | <1.071                           | 0.833                           | <0.938                           | ns       | 35,36 |
| Average high pulse width  | tCH(avg)       | 0.48   | 0.52                             | 0.48                            | 0.52                             | 0.48                            | 0.52                             | tCK(avg) |       |
| Average low pulse width   | tCL(avg)       | 0.48   | 0.52                             | 0.48                            | 0.52                             | 0.48                            | 0.52                             | tCK(avg) |       |
| Absolute Clock Period   | tCK(abs)       | tCK(avg)min + tJIT(per)min_to t  | tCK(avg)m ax + tJIT(per)m ax_tot | tCK(avg)min + tJIT(per)min_to t | tCK(avg)m ax + tJIT(per)m ax_tot | tCK(avg)min + tJIT(per)min_to t | tCK(avg)m ax + tJIT(per)m ax_tot | tCK(avg) |       |
| Absolute clock HIGH pulse width   | tCH(abs)       | 0.45   | -                                | 0.45                            | -                                | 0.45                            | -                                | tCK(avg) | 23    |
| Absolute clock LOW pulse width  | tCL(abs)       | 0.45   | -                                | 0.45                            | -                                | 0.45                            | -                                | tCK(avg) | 24    |
| Clock Period Jitter- total  | JIT(per)_tot   | -54  | 54                               | -47                             | 47                               | -42                             | 42                               | ps       | 23    |
| Clock Period Jitter- deterministic  | JIT(per)_dj    | -27  | 27                               | -23                             | 23                               | -21                             | 21                               | ps       | 26    |
| Clock Period Jitter during DLL locking period                                       | tJIT(per, lck) | -43  | 43                               | -38                             | 38                               | -33                             | 33                               | ps       |       |
| Cycle to Cycle Period Jitter  | tJIT(cc)_total | 107  |                                  | 94                              |                                  | 83                              |                                  | ps       | 25    |
| Cycle to Cycle Period Jitter deterministic  | tJIT(cc)_dj    | 54   |                                  | 47                              |                                  | 42                              |                                  | ps       | 26    |
| Cycle to Cycle Period Jitter during DLL locking period                              | tJIT(cc, lck)  | 86   |                                  | 75                              |                                  | 67                              |                                  | ps       |       |
| Duty Cycle Jitter   | tJIT(duty)     | TBD  | TBD                              | TBD                             | TBD                              | TBD                             | TBD                              | ps       |       |
| Cumulative error across 2 cycles  | tERR(2per)     | -79  | 79                               | -69                             | 69                               | -61                             | 61                               | ps       |       |
| Cumulative error across 3 cycles  | tERR(3per)     | -94  | 94                               | -82                             | 82                               | -73                             | 73                               | ps       |       |
| Cumulative error across 4 cycles  | tERR(4per)     | -104   | 104                              | -91                             | 91                               | -81                             | 81                               | ps       |       |
| Cumulative error across 5 cycles  | tERR(5per)     | -112   | 112                              | -98                             | 98                               | -87                             | 87                               | ps       |       |
| Cumulative error across 6 cycles  | tERR(6per)     | -119   | 119                              | -104                            | 104                              | -92                             | 92                               | ps       |       |
| Cumulative error across 7 cycles  | tERR(7per)     | -124   | 124                              | -109                            | 109                              | -97                             | 97                               | ps       |       |
| Cumulative error across 8 cycles  | tERR(8per)     | -129   | 129                              | -113                            | 113                              | -101                            | 101                              | ps       |       |
| Cumulative error across 9 cycles  | tERR(9per)     | -134   | 134                              | -117                            | 117                              | -104                            | 104                              | ps       |       |
| Cumulative error across 10 cycles   | tERR(10per)    | -137   | 137                              | -120                            | 120                              | -107                            | 107                              | ps       |       |
| Cumulative error across 11 cycles   | tERR(11per)    | -141   | 141                              | -123                            | 123                              | -110                            | 110                              | ps       |       |
| Cumulative error across 12 cycles   | tERR(12per)    | -144   | 144                              | -126                            | 126                              | -112                            | 112                              | ps       |       |
| Cumulative error across 13 cycles   | tERR(13per)    | -147   | 147                              | -129                            | 129                              | -114                            | 114                              | ps       |       |
| Cumulative error across 14 cycles   | tERR(14per)    | -150   | 150                              | -131                            | 131                              | -116                            | 116                              | ps       |       |
| Cumulative error across 15 cycles   | tERR(15per)    | -152   | 152                              | -133                            | 133                              | -118                            | 118                              | ps       |       |
| Cumulative error across 16 cycles   | tERR(16per)    | -155   | 155                              | -135                            | 135                              | -120                            | 120                              | ps       |       |
| Cumulative error across 17 cycles   | tERR(17per)    | -157   | 157                              | -137                            | 137                              | -122                            | 122                              | ps       |       |
| Cumulative error across 18 cycles   | tERR(18per)    | -159   | 159                              | -139                            | 139                              | -124                            | 124                              | ps       |       |
| Cumulative error across n = 13, 14 . . . 49, 50 cycles                              | tERR(nper)     | $tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min)$<br>$tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)$ |                                  |                                 |                                  |                                 |                                  | ps       |       |
| Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels | tIS(base)      | 100  | -                                | 80                              | -                                | 62                              | -                                | ps       |       |
| Command and Address setup time to CK_t, CK_c referenced to Vref levels              | tIS(Vref)      | 200  | -                                | 180                             | -                                | 162                             | -                                | ps       |       |
| Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels  | tIH(base)      | 125  | -                                | 105                             | -                                | 87                              | -                                | ps       |       |

| Speed   |               | DDR4-1866                                 |     | DDR4-2133               |     | DDR4-2400               |     | Units | NOTE      |
|---|---------------|---|-----|-------------------------|-----|-------------------------|-----|-------|-----------|
| Parameter   | Symbol        | MIN                                       | MAX | MIN                     | MAX | MIN                     | MAX |       |           |
| <b>Command and Address Timing</b>   |               |   |     |                         |     |                         |     |       |           |
| Command and Address hold time to CK <sub>t</sub> , CK <sub>c</sub> referenced to Vref levels                                  | tIH(Vref)     | 200                                       | -   | 180                     | -   | 162                     | -   | ps    |           |
| Control and Address Input pulse width for each input  | tIPW          | 525                                       | -   | 460                     | -   | 410                     | -   | ps    |           |
| CAS <sub>n</sub> to CAS <sub>n</sub> command delay for same bank group  | tCCD_L        | 5   | -   | 6                       | -   | 6                       | -   | nCK   | 34        |
| CAS <sub>n</sub> to CAS <sub>n</sub> command delay for different bank group   | tCCD_S        | 4   | -   | 4                       | -   | 4                       | -   | nCK   | 34        |
| ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size  | tRRD_S(2K)    | Max(4nCK,5.3ns)                           | -   | Max(4nCK,5.3ns)         | -   | Max(4nCK,5.3ns)         | -   | nCK   | 34        |
| ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size  | tRRD_S(1K)    | Max(4nCK,4.2ns)                           | -   | Max(4nCK,3.7ns)         | -   | Max(4nCK,3.3ns)         | -   | nCK   | 34        |
| ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size  | tRRD_S(1/2K)  | Max(4nCK,4.2ns)                           | -   | Max(4nCK,3.7ns)         | -   | Max(4nCK,3.3ns)         | -   | nCK   | 34        |
| ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size   | tRRD_L(2K)    | Max(4nCK,6.4ns)                           | -   | Max(4nCK,6.4ns)         | -   | Max(4nCK,6.4ns)         | -   | nCK   | 34        |
| ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size   | tRRD_L(1K)    | Max(4nCK,5.3ns)                           | -   | Max(4nCK,5.3ns)         | -   | Max(4nCK,4.9ns)         | -   | nCK   | 34        |
| ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size   | tRRD_L(1/2K)  | Max(4nCK,5.3ns)                           | -   | Max(4nCK,5.3ns)         | -   | Max(4nCK,4.9ns)         | -   | nCK   | 34        |
| Four activate window for 2KB page size  | tFAW_2K       | Max(28nCK,30ns)                           | -   | Max(28nCK,30ns)         | -   | Max(28nCK,30ns)         | -   | ns    | 34        |
| Four activate window for 1KB page size  | tFAW_1K       | Max(20nCK,23ns)                           | -   | Max(20nCK,21ns)         | -   | Max(20nCK,21ns)         | -   | ns    | 34        |
| Four activate window for 1/2KB page size  | tFAW_1/2K     | Max(16nCK,17ns)                           | -   | Max(16nCK,15ns)         | -   | Max(16nCK,13ns)         | -   | ns    | 34        |
| Delay from start of internal write transaction to internal read command for different bank group                              | tWTR_S        | max(2nCK,2.5ns)                           | -   | max(2nCK,2.5ns)         | -   | max(2nCK,2.5ns)         | -   |       | 1,2,e,3,4 |
| Delay from start of internal write transaction to internal read command for same bank group                                   | tWTR_L        | max(4nCK,7.5ns)                           | -   | max(4nCK,7.5ns)         | -   | max(4nCK,7.5ns)         | -   |       | 1,3,4     |
| Internal READ Command to PRE-CHARGE Command delay   | tRTP          | max(4nCK,7.5ns)                           | -   | max(4nCK,7.5ns)         | -   | max(4nCK,7.5ns)         | -   |       |           |
| WRITE recovery time   | tWR           | 15  | -   | 15                      | -   | 15                      | -   | ns    | 1         |
| Write recovery time when CRC and DM are enabled   | tWR_CRC DM    | tWR+max(5nCK,3.75ns)                      | -   | tWR+max(5nCK,3.75ns)    | -   | tWR+max(5nCK,3.75ns)    | -   | ns    | 1, 28     |
| delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled | tWTR_S_CRC DM | tWTR_S+max(5nCK,3.75ns)                   | -   | tWTR_S+max(5nCK,3.75ns) | -   | tWTR_S+max(5nCK,3.75ns) | -   | ns    | 2, 29, 34 |
| delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled      | tWTR_L_CRC DM | tWTR_L+max(5nCK,3.75ns)                   | -   | tWTR_L+max(5nCK,3.75ns) | -   | tWTR_L+max(5nCK,3.75ns) | -   | ns    | 3,30, 34  |
| DLL locking time  | tDLLK         | 597                                       | -   | 768                     | -   | 768                     | -   | nCK   |           |
| Mode Register Set command cycle time  | tMRD          | 8   | -   | 8                       | -   | 8                       | -   | nCK   |           |
| Mode Register Set command update delay  | tMOD          | max(24nCK,15ns)                           | -   | max(24nCK,15ns)         | -   | max(24nCK,15ns)         | -   |       |           |
| Multi-Purpose Register Recovery Time  | tMPRR         | 1   | -   | 1                       | -   | 1                       | -   | nCK   | 33        |
| Multi Purpose Register Write Recovery Time  | tWR_MPR       | tMOD (min) + AL + PL                      | -   | tMOD (min) + AL + PL    | -   | tMOD (min) + AL + PL    | -   | -     |           |
| Auto precharge write recovery + precharge time  | tDAL(min)     | Programmed WR + roundup ( tRP / tCK(avg)) |     |                         |     |                         |     | nCK   |           |
| <b>CS<sub>n</sub> to Command Address Latency</b>  |               |   |     |                         |     |                         |     |       |           |
| CS <sub>n</sub> to Command Address Latency  | tCAL          | 4   |     |                         |     |                         |     | -     | 4         |

| Speed   |          | DDR4-1866               |      | DDR4-2133               |      | DDR4-2400                |      | Units        | NOTE     |
|---|----------|-------------------------|------|-------------------------|------|--------------------------|------|--------------|----------|
| Parameter   | Symbol   | MIN                     | MAX  | MIN                     | MAX  | MIN                      | MAX  |              |          |
| <b>DRAM Data Timing</b>   |          |                         |      |                         |      |                          |      |              |          |
| DQS <sub>t</sub> , DQS <sub>c</sub> to DQ skew, per group, per access   | tDQSQ    | -                       | TBD  | -                       | TBD  | -                        | TBD  | tCK(avg) / 2 | 13,18    |
| DQS <sub>t</sub> , DQS <sub>c</sub> to DQ Skew deterministic, per group, per access                                 | tDQSQ    | -                       | TBD  | -                       | TBD  | -                        | TBD  | tCK(avg) / 2 | 14,16,18 |
| DQ output hold time from DQS <sub>t</sub> , DQS <sub>c</sub>  | tQH      | TBD                     | -    | TBD                     | -    | TBD                      | -    | tCK(avg) / 2 | 13,17,18 |
| DQ output hold time deterministic from DQS <sub>t</sub> , DQS <sub>c</sub>  | tQH      | TBD                     | -    | TBD                     | -    | TBD                      | -    | UI           | 14,16,18 |
| DQS <sub>t</sub> , DQS <sub>c</sub> to DQ Skew total, per group, per access; DBI enabled                            | tDQSQ    | -                       | TBD  | -                       | TBD  | -                        | TBD  | UI           | 13,19    |
| DQ output hold time total from DQS <sub>t</sub> , DQS <sub>c</sub> ; DBI enabled                                    | tQH      | TBD                     | -    | TBD                     | -    | TBD                      | -    | UI           | 13,19    |
| DQ to DQ offset, per group, per access referenced to DQS <sub>t</sub> , DQS <sub>c</sub>                            | tDQSQ    | TBD                     | TBD  | TBD                     | TBD  | TBD                      | TBD  | UI           | 15,16    |
| <b>Data Strobe Timing</b>   |          |                         |      |                         |      |                          |      |              |          |
| DQS <sub>t</sub> , DQS <sub>c</sub> differential READ Preamble (2 clock preamble)                                   | tRPRE    | 0.9                     | TBD  | 0.9                     | TBD  | 0.9                      | TBD  | tCK          |          |
| DQS <sub>t</sub> , DQS <sub>c</sub> differential READ Postamble   | tRPST    | TBD                     | TBD  | TBD                     | TBD  | TBD                      | TBD  | tCK          |          |
| DQS <sub>t</sub> , DQS <sub>c</sub> differential output high time   | tQSH     | 0.4                     | -    | 0.4                     | -    | 0.4                      | -    | tCK          | 21       |
| DQS <sub>t</sub> , DQS <sub>c</sub> differential output low time  | tQSL     | 0.4                     | -    | 0.4                     | -    | 0.4                      | -    | tCK          | 20       |
| DQS <sub>t</sub> , DQS <sub>c</sub> differential WRITE Preamble   | tWPRE    | 0.9                     | -    | 0.9                     | -    | 0.9                      | -    | tCK          |          |
| DQS <sub>t</sub> , DQS <sub>c</sub> differential WRITE Postamble  | tWPST    | TBD                     | TBD  | TBD                     | TBD  | TBD                      | TBD  | tCK          |          |
| DQS <sub>t</sub> and DQS <sub>c</sub> low-impedance time (Referenced from RL-1)                                     | tLZ(DQS) | -390                    | 195  | -360                    | 180  | -300                     | 150  | ps           |          |
| DQS <sub>t</sub> and DQS <sub>c</sub> high-impedance time (Referenced from RL+BL/2)                                 | tHZ(DQS) | -                       | 195  | -                       | 180  | -                        | 150  | ps           |          |
| DQS <sub>t</sub> , DQS <sub>c</sub> differential input low pulse width  | tDQSL    | 0.46                    | 0.54 | 0.46                    | 0.54 | 0.46                     | 0.54 | tCK          |          |
| DQS <sub>t</sub> , DQS <sub>c</sub> differential input high pulse width   | tDQSH    | 0.46                    | 0.54 | 0.46                    | 0.54 | 0.46                     | 0.54 | tCK          |          |
| DQS <sub>t</sub> , DQS <sub>c</sub> rising edge to CK <sub>t</sub> , CK <sub>c</sub> rising edge (1 clock preamble) | tDQSS    | -0.27                   | 0.27 | -0.27                   | 0.27 | -0.27                    | 0.27 | tCK          |          |
| DQS <sub>t</sub> , DQS <sub>c</sub> falling edge setup time to CK <sub>t</sub> , CK <sub>c</sub> rising edge        | tDSS     | 0.18                    | -    | 0.18                    | -    | 0.18                     | -    | tCK          |          |
| DQS <sub>t</sub> , DQS <sub>c</sub> falling edge hold time from CK <sub>t</sub> , CK <sub>c</sub> rising edge       | tDSH     | 0.18                    | -    | 0.18                    | -    | 0.18                     | -    | tCK          |          |
| <b>MPSM Timing</b>  |          |                         |      |                         |      |                          |      |              |          |
| Command path disable delay upon MPSM entry  | tMPED    | tMOD(min) + tCPDED(min) | -    | tMOD(min) + tCPDED(min) | -    | tMOD(min) + tCP-DED(min) | -    |              |          |
| Valid clock requirement after MPSM entry  | tCKMPE   | tMOD(min) + tCPDED(min) | -    | tMOD(min) + tCPDED(min) | -    | tMOD(min) + tCP-DED(min) | -    |              |          |
| Valid clock requirement before MPSM exit  | tCKMPX   | tCKSRX(min)             |      | tCKSRX(min)             |      | tCK- SRX(min)            | -    |              |          |
| Exit MPSM to commands not requiring a locked DLL  | tXMP     | TBD                     |      | TBD                     |      | TBD                      | -    |              |          |
| Exit MPSM to commands requiring a locked DLL  | tXMPDLL  | tXMP(min) + tXSDLL(min) |      | tXMP(min) + tXSDLL(min) |      | tXMP(min) + tXSDLL(min)  | -    |              |          |
| CS setup time to CKE  | tMPX_S   | TBD                     | -    | TBD                     | -    | TBD                      | -    |              |          |
| CS hold time to CKE   | tMPX_H   | TBD                     | -    | TBD                     | -    | TBD                      | -    |              |          |

| Speed   |                 | DDR4-1866           |         | DDR4-2133           |         | DDR4-2400           |         | Units | NOTE  |
|---|-----------------|---------------------|---------|---------------------|---------|---------------------|---------|-------|-------|
| Parameter   | Symbol          | MIN                 | MAX     | MIN                 | MAX     | MIN                 | MAX     |       |       |
| <b>Calibration Timing</b>   |                 |                     |         |                     |         |                     |         |       |       |
| Power-up and RESET calibration time   | tZQinit         | 1024                | -       | 1024                | -       | 1024                | -       | nCK   |       |
| Normal operation Full calibration time  | tZQoper         | 512                 | -       | 512                 | -       | 512                 | -       | nCK   |       |
| Normal operation Short calibration time   | tZQCS           | 128                 | -       | 128                 | -       | 128                 | -       | nCK   |       |
| <b>Reset/Self Refresh Timing</b>  |                 |                     |         |                     |         |                     |         |       |       |
| Exit Reset from CKE HIGH to a valid   | tXPR            | max (5nCK,tRFC)     | -       | max (5nCK,tRFC)     | -       | max (5nCK,tRFC)     | -       |       |       |
| Exit Self Refresh to commands not requiring a locked DLL  | tXS             | tRFC(min)+10ns      | -       | tRFC(min)+10ns      | -       | tRFC(min)+10ns      | -       |       |       |
| SRX to commands not requiring a locked DLL in Self Refresh ABORT  | tXS_ABORT (min) | tRFC4(min)+10ns     | -       | tRFC4(min)+10ns     | -       | tRFC4(min)+10ns     | -       |       |       |
| Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)  | tXS_FAST (min)  | tRFC4(min)+10ns     | -       | tRFC4(min)+10ns     | -       | tRFC4(min)+10ns     | -       |       |       |
| Exit Self Refresh to commands requiring a locked DLL  | tXSDLL          | tDLLK(min)          | -       | tDLLK(min)          | -       | tDLLK(min)          | -       |       |       |
| Minimum CKE low width for Self refresh entry to exit timing   | tCKESR          | tCKE(min)+1nCK      | -       | tCKE(min)+1nCK      | -       | tCKE(min)+1nCK      | -       |       |       |
| Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled  | tCKESR_PAR      | tCKE(min)+1nCK+PL   | -       | tCKE(min)+1nCK+PL   | -       | tCKE(min)+1nCK+PL   | -       |       |       |
| Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)  | tCKSRE          | max(5nCK,10ns)      | -       | max(5nCK,10ns)      | -       | max(5nCK,10ns)      | -       |       |       |
| Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled                                    | tCKSRE_PARR     | max(5nCK,10ns)+PL   | -       | max(5nCK,10ns)+PL   | -       | max(5nCK,10ns)+PL   | -       |       |       |
| Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit                                     | tCKSRX          | max(5nCK,10ns)      | -       | max(5nCK,10ns)      | -       | max(5nCK,10ns)      | -       |       |       |
| <b>Power Down Timing</b>  |                 |                     |         |                     |         |                     |         |       |       |
| Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL | tXP             | max (4nCK,6ns)      | -       | max (4nCK,6ns)      | -       | max (4nCK,6ns)      | -       |       |       |
| CKE minimum pulse width   | tCKE            | max (3nCK, 5ns)     | -       | max (3nCK, 5ns)     | -       | max (3nCK, 5ns)     | -       |       | 31,32 |
| Command pass disable delay  | tCPDED          | 4                   | -       | 4                   | -       | 4                   | -       | nCK   |       |
| Power Down Entry to Exit Timing   | tPD             | tCKE(min)           | 9*tREFI | tCKE(min)           | 9*tREFI | tCKE(min)           | 9*tREFI |       | 6     |
| Timing of ACT command to Power Down entry   | tACTPDEN        | 1                   | -       | 2                   | -       | 2                   | -       | nCK   | 7     |
| Timing of PRE or PREA command to Power Down entry   | tPRPDEN         | 1                   | -       | 2                   | -       | 2                   | -       | nCK   | 7     |
| Timing of RD/RDA command to Power Down entry  | tRDPDEN         | RL+4+1              | -       | RL+4+1              | -       | RL+4+1              | -       | nCK   |       |
| Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)   | tWRPDEN         | WL+4+(tWR/tCK)(avg) | -       | WL+4+(tWR/tCK)(avg) | -       | WL+4+(tWR/tCK)(avg) | -       | nCK   | 4     |
| Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)  | tWRAPDEN        | WL+4+WR+1           | -       | WL+4+WR+1           | -       | WL+4+WR+1           | -       | nCK   | 5     |
| Timing of WR command to Power Down entry (BC4MRS)   | tWRPBC4DEN      | WL+2+(tWR/tCK)(avg) | -       | WL+2+(tWR/tCK)(avg) | -       | WL+2+(tWR/tCK)(avg) | -       | nCK   | 4     |
| Timing of WRA command to Power Down entry (BC4MRS)  | tWRAPBC4DEN     | WL+2+WR+1           | -       | WL+2+WR+1           | -       | WL+2+WR+1           | -       | nCK   | 5     |
| Timing of REF command to Power Down entry   | tREFPDEN        | 1                   | -       | 2                   | -       | 2                   | -       | nCK   | 7     |

| Speed   |                  | DDR4-1866       |        | DDR4-2133       |        | DDR4-2400       |        | Units    | NOTE |
|---|------------------|-----------------|--------|-----------------|--------|-----------------|--------|----------|------|
| Parameter   | Symbol           | MIN             | MAX    | MIN             | MAX    | MIN             | MAX    |          |      |
| Timing of MRS command to Power Down entry   | tMRSPDEN         | tMOD(min)       | -      | tMOD(min)       | -      | tMOD(min)       | -      |          |      |
| <b>PDA Timing</b>   |                  |                 |        |                 |        |                 |        |          |      |
| Mode Register Set command cycle time in PDA mode  | tMRD_PDA         | max(16nCK,10ns) |        | max(16nCK,10ns) |        | max(16nCK,10ns) |        |          |      |
| Mode Register Set command update delay in PDA mode  | tMOD_PDA         | tMOD            |        | tMOD            |        | tMOD            |        |          |      |
| <b>ODT Timing</b>   |                  |                 |        |                 |        |                 |        |          |      |
| Asynchronous RTT turn-on delay (Power-Down with DLL frozen)   | tAONAS           | 1.0             | 9.0    | 1.0             | 9.0    | 1.0             | 9.0    | ns       |      |
| Asynchronous RTT turn-off delay (Power-Down with DLL frozen)  | tAOFAS           | 1.0             | 9.0    | 1.0             | 9.0    | 1.0             | 9.0    | ns       |      |
| RTT dynamic change skew   | tADC             | 0.3             | 0.7    | 0.3             | 0.7    | 0.3             | 0.7    | tCK(avg) |      |
| <b>Write Leveling Timing</b>  |                  |                 |        |                 |        |                 |        |          |      |
| First DQS_t/DQS_n rising edge after write leveling mode is programmed   | tWLMRD           | 40              | -      | 40              | -      | 40              | -      | nCK      | 12   |
| DQS_t/DQS_n delay after write leveling mode is programmed   | tWLDQSEN         | 25              | -      | 25              | -      | 25              | -      | nCK      | 12   |
| Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/ DQS_n                                | tWLS             | 0.13            | -      | 0.13            | -      | 0.13            | -      | tCK(avg) |      |
| Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t  | tWLH             | 0.13            | -      | 0.13            | -      | 0.13            | -      | tCK(avg) |      |
| Write leveling output delay   | tWLO             | 0               | 9.5    | 0               | 9.5    | 0               | 9.5    | ns       |      |
| Write leveling output error   | tWLOE            |                 |        |                 |        |                 |        | ns       |      |
| <b>CA Parity Timing</b>   |                  |                 |        |                 |        |                 |        |          |      |
| Commands not guaranteed to be executed during this time   | tPAR_UNKNOWN     | -               | PL     | -               | PL     | -               | PL     |          |      |
| Delay from errant command to ALERT_n assertion  | tPAR_ALERT_n     | -               | PL+6ns | -               | PL+6ns | -               | PL+6ns |          |      |
| Pulse width of ALERT_n signal when asserted   | tPAR_ALERT_n_PW  | 56              | 112    | 64              | 128    | 72              | 144    | nCK      |      |
| Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode | tPAR_ALERT_n_RSP | -               | 50     | -               | 57     | -               | 64     | nCK      |      |
| Parity Latency  | PL               | 4               |        | 4               |        | 5               |        | nCK      |      |
| <b>CRC Error Reporting</b>  |                  |                 |        |                 |        |                 |        |          |      |
| CRC error to ALERT_n latency  | tCRC_ALERT_n     | 3               | 13     | 3               | 13     | 3               | 13     | ns       |      |
| CRC ALERT_n pulse width   | CRC_ALERT_n_PW   | 6               | 10     | 6               | 10     | 6               | 10     | nCK      |      |
| <b>tREFI</b>  |                  |                 |        |                 |        |                 |        |          |      |
| tRFC1 (min)   | 2Gb              | 160             | -      | 160             | -      | 160             | -      | ns       | 34   |
|   | 4Gb              | 260             | -      | 260             | -      | 260             | -      | ns       | 34   |
|   | 8Gb              | 350             | -      | 350             | -      | 350             | -      | ns       | 34   |
|   | 16Gb             | TBD             | -      | TBD             | -      | TBD             | -      | ns       | 34   |
| tRFC2 (min)   | 2Gb              | 110             | -      | 110             | -      | 110             | -      | ns       | 34   |
|   | 4Gb              | 160             | -      | 160             | -      | 160             | -      | ns       | 34   |
|   | 8Gb              | 260             | -      | 260             | -      | 260             | -      | ns       | 34   |
|   | 16Gb             | TBD             | -      | TBD             | -      | TBD             | -      | ns       | 34   |
| tRFC4 (min)   | 2Gb              | 90              | -      | 90              | -      | 90              | -      | ns       | 34   |
|   | 4Gb              | 110             | -      | 110             | -      | 110             | -      | ns       | 34   |
|   | 8Gb              | 160             | -      | 160             | -      | 160             | -      | ns       | 34   |
|   | 16Gb             | TBD             | -      | TBD             | -      | TBD             | -      | ns       | 34   |

**Note:**

1. Start of internal write transaction is defined as follows :  
For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL. For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.  
For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TOPER.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down  
IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports  $tnPARAM[nCK]=RU\{tPARAM[ns]/tCK(avg)[ns]\}$ , which is in clock cycles assuming all input clock jitter specifications are satisfied
9. When CRC and DM are both enabled, tWR\_CRC\_DM is used in place of tWR.
10. When CRC and DM are both enabled tWTR\_S\_CRC\_DM is used in place of tWTR\_S.
11. When CRC and DM are both enabled tWTR\_L\_CRC\_DM is used in place of tWTR\_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
14. The deterministic component of the total timing. Measurement method tbd.
15. DQ to DQ static offset relative to strobe per group. Measurement method tbd.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual  $tjit(per)_{total}$  of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS\_t - DQS\_c, as measured from on falling edge to the next consecutive rising edge
21. tQSH describes the instantaneous differential output high pulse width on DQS\_t - DQS\_c, as measured from on falling edge to the next consecutive rising edge
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR\_CRC\_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR\_S\_CRC\_DM is used in place of tWTR\_S.
30. When CRC and DM are both enabled tWTR\_L\_CRC\_DM is used in place of tWTR\_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification ( Low pulse width ).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification ( HIGH pulse width ).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables shown in section 10.
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.  $UI=tCK(avg).min/2$

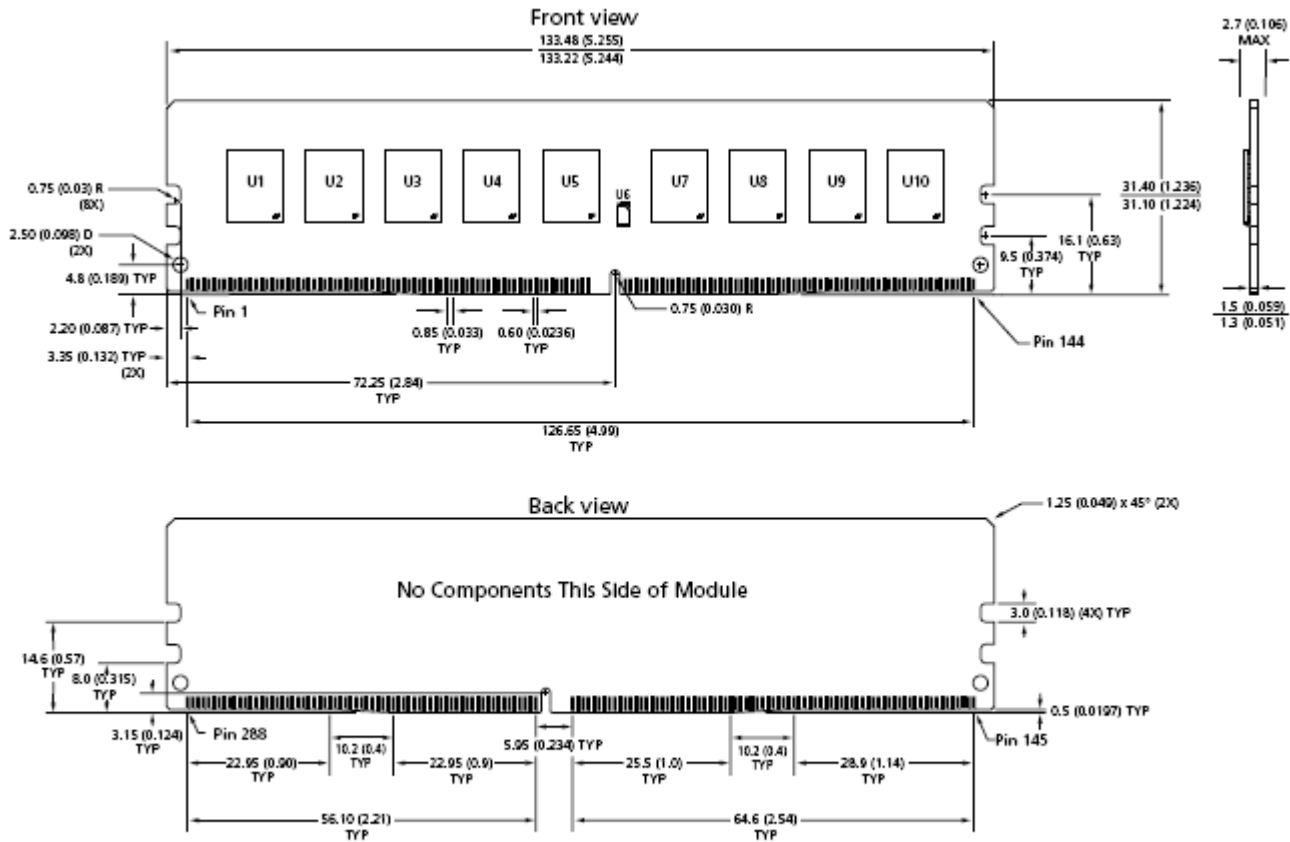


## 288-pin ECC-UDIMM

## DDR4 SDRAM

### 14. Physical Dimensions: 1Gx72 Single Rank x8 (1Gx8 base)

Unit: Millimeters



- Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.  
2. The dimensional diagram is for reference only.

\* NOTE : Tolerances on all dimensions  $\pm 0.15$  unless otherwise specified.