DDR4 OverClock UDIMM Module

4GB based on 4Gbit component

TFBGA with Pb-Free

Revision 1.0 (May. 2016)
-Initial Release

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SUPER*TALENT DDR4 OverClock Series is specifically designed for games and Overclock Alike for Extrem overclocking performance.
Built-in XMP 2.0 support gives you trouble-free, automatic overclocking
SuperTalent strictly adheres to quality standards set by JEDEC and ISO9001 .
With 100% tested in multiple PC majoy-brand motherboard environments at its rated speed and latency.SuperTalent makes sure both stability and performance of every module reach the highest quality criteria.

1. Features

- Low latency and fast speeds deliver superior performance.
- 288-pin, unbuffered dual in-line memory module(UDIMM)
- Fast data transfer rates: DDR4-3733, DDR4-3600 ,DDR4-3466, DDR4-3200 or DDR4-3000
- Programmable CAS Latency(posted CAS): CL 15-17
- Organization : 4GB (512M x 64) , by 4Gb(512Mx8) ,8Pcs chips
- Intel XMP 2.0
- VDD Voltage: 1.35V (XMP) and 1.20V (standard)
- VDDSPD = 2.5V (NOM)
- Nominal and dynamic on-die termination (ODT) fordata, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Single-rank/1 rank
- On-board I2 serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each
- Gold edge contacts
- With Heatsink
- Halogen-free,ROSH complian

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2. Ordering Information and Key Features

Part Number	Density	Speed/Frequency	CL-tRCD-tRP-tRAS	Voltage	tCK(min)
F3733UA4G	4GB	DDR4-3733 MHz	17-19-19-39	1.35V	0.536ns
F3600UA4G	4GB	DDR4-3600 MHz	17-18-18-38	1.35V	0.555ns
F3466UA4G	4GB	DDR4-3466 MHz	16-18-18-36	1.35V	0.577ns
F3200UA4G	4GB	DDR4-3200 MHz	16-18-18-36	1.35V	0.625ns
F3000UA4G	4GB	DDR4-3000 MHz	15-16-16-35	1.35V	0.666ns

Note1 : All Part Number with JEDEC standard speed and latency : **DDR4-2133 15-15-15-35 1.2V voltage.**

Note2 : Before Purchase and Assembly your computer,please consult motherboard and CPU manufacture, review the motherboard and CPU manufacture website,Check the hardware Spec, make sure the hardware support the memory module rated speed and latency.

3. Addressing

Parameter	4GB
Row address	32K A[14:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	4Gb (512 Meg x 8), 16 banks
Module rank address	CS0_n

4. Absolute Maximum DC Rating

Symbol	Parameter	Rating	Units
V_{DD}	Voltage on VDD pin relative to Vss	-0.4 ~ 1.5	V
V_{DDQ}	Voltage on VDDQ pin relative to Vss	-0.4 ~ 1.5	V
VPP	Voltage on VPP pin relative to Vss	-0.4 ~ 3.0	V
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA to Vss	-0.4 ~ 1.5	V
T_{STG}	Storage Temperature	-55 ~ + 100	℃
TOPER	Normal operating temperature range	0 ~ + 85	℃

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5. Connector Pinout and Signal Description

Pin Name	Description	Pin Name	Description
A0–A17[1]	SDRAM address bus	SCL	I^2C serial bus clock for SPD-TSE
BA0, BA1	SDRAM bank select	SDA	I^2C serial bus data line for SPD-TSE
BG0, BG1	SDRAM bank group select	SA0–SA2	I^2C slave address select for SPD-TSE
RAS_n[2]	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n[3]	SDRAM column address strobe	VDD	SDRAM I/O and core power supply
WE_n[4]	SDRAM write enable	C0, C1, C2	Chip ID lines
CS0_n, CS1_n	DIMM Rank Select Lines	12 V	Optional power Supply on socket but not used on UDIMM
CKE0, CKE1	SDRAM clock enable lines	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	SDRAM on-die termination control lines	VSS	Power supply return (ground)
ACT_n	SDRAM activate	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS0_t-TDQS8_t TDQS0_c-TDQS8_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs. Not used on UDIMMs.		
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)		
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)	RESET_n	Set DRAMs to a Known State
DM0_n–DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inversion (x8-based x72 DIMMs)	EVENT_n	SPD signals a thermal event has occurred.
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)	VTT	SDRAM I/O termination supply
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)	RFU	Reserved for future use

Note 1 Address A17 is not valid for x8 and x16 based SDRAMs. For UDIMMs, this connection pin is NC.
Note 2 RAS_n is a multiplexed function with A16.
Note 3 CAS_n is a multiplexed function with A15.
Note 4 WE_n is a multiplexed function with A14.

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6. Input/Output Functional Description

Symbol	Type	Function
CK0_t, CK0_c, CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS2_n and CS3_n are not used on UDIMMs.
C0, C1, C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code. Not used on UDIMMs.
ODT0, ODT1	Input	On-Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration, ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15, and A14, but for non-activation command with ACT_n High, these are Command pins for Read, Write, and other commands defined in the command truth table.
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations. TDQS is not valid for UDIMMs.
BG0, BG1	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write, or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/x8 SDRAM configurations have BG0 and BG1. x16 based SDRAMs only have BG0.
BA0, BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 SDRAM configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.

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7. Input/Output Functional Description (Cont'd)

Symbol	Type	Function
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c are not valid for UDIMMs.
PARITY	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A16-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Output	Alert: It has multiple functions, such as CRC error flag, Command and Address Parity error flag, as an Output signal. If there is an error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is an error in Command Address Parity Check, then ALERT_n goes LOW for a relatively long period until the on-going DRAM internal recovery transaction is complete. During Connectivity Test mode, this pin functions as an input. Using this signal or not is dependent on the system.
RFU		Reserved for Future Use. No on DIMM electrical connection is present.
NC		No Connect: No on DIMM electrical connection is present.
VDD[1]	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VTT[2]	Supply	Power Supply for termination of Address, Command and Control, VDD/2.
12 V	Supply	12 V supply not used on UDIMMs.
VDDSPD	Supply	Power supply used to power the I2C bus on the SPD-TSE.
VREFCA	Supply	Reference voltage for CA

Note 1 For PC4 VDD 1.2 V. For PC4L VDD is TBD.
Note 2 For PC4 VTT is 0.60 V. For PC4L VTT is TBD.

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8. DDR4 288 Pin UDIMM Pin Wiring Assignments

Front Side Pin Label	Pin	Pin	Back side Pin Label
12 V, NC	1	145	*12 V,* NC
VSS	2	146	VREFCA
DQ4	3	147	VSS
VSS	4	148	DQ5
DQ0	5	149	VSS
VSS	6	150	DQ1
TDQS9_t, DQS9_t, DM0_n, DBI0_n, NC	7	151	VSS
TDQS9_c, DQS9_c, NC	8	152	DQS0_c
VSS	9	153	DQS0_t
DQ6	10	154	VSS
VSS	11	155	DQ7
DQ2	12	156	VSS
VSS	13	157	DQ3
DQ12	14	158	VSS
VSS	15	159	DQ13
DQ8	16	160	VSS
VSS	17	161	DQ9
TDQS10_t, DQS10_t, DM1_n, DBI1_n, NC	18	162	VSS
TDQS10_c, DQS10_c, NC	19	163	DQS1_c
VSS	20	164	DQS1_t
DQ14	21	165	VSS
VSS	22	166	DQ15
DQ10	23	167	VSS
VSS	24	168	DQ11
DQ20	25	169	VSS
VSS	26	170	DQ21
DQ16	27	171	VSS
VSS	28	172	DQ17
TDQS11_t, DQS11_t, DM2_n, DBI2_n, NC	29	173	VSS
TDQS11_c, DQS11_c, NC	30	174	DQS2_c
VSS	31	175	DQS2_t
DQ22	32	176	VSS
VSS	33	177	DQ23
DQ18	34	178	VSS
VSS	35	179	DQ19
DQ28	36	180	VSS
VSS	37	181	DQ29
DQ24	38	182	VSS
VSS	39	183	DQ25
TDQS12_t, DQS12_t, DM3_n, DBI3_n, NC	40	184	VSS
TDQS12_c, DQS12_c, NC	41	185	DQS3_c
VSS	42	186	DQS3_t
DQ30	43	187	VSS
VSS	44	188	DQ31
DQ26	45	189	VSS
VSS	46	190	DQ27
CB4, NC	47	191	VSS

Front Side Pin Label	Pin	Pin	Back side Pin Label
CK0_t	74	218	CK1_t
CK0_c	75	219	CK1_c
VDD	76	220	VDD
VTT	77	221	VTT
	KEY		
EVENT_n	78	222	PARITY
A0	79	223	VDD
VDD	80	224	BA1
BA0	81	225	A10/AP
RAS_n/A16	82	226	VDD
VDD	83	227	RFU
CS0_n	84	228	WE_n/A14
VDD	85	229	VDD
CAS_n/A15	86	230	NC*, SAVE_n*
ODT0	87	231	VDD
VDD	88	232	A13
CS1_n	89	233	VDD
VDD	90	234	NC*, A17*
ODT1	91	235	NC*, C2*
VDD	92	236	VDD
C0, CS2_n, NC	93	237	NC*, CS3_n,*
VSS	94	238	SA2
DQ36	95	239	VSS
VSS	96	240	DQ37
DQ32	97	241	VSS
VSS	98	242	DQ33
TDQS13_t, DQS13_t, DM4_n, DBI4_n, NC	99	243	VSS
TDQS13_c, DQS13_c, NC	100	244	DQS4_c
VSS	101	245	DQS4_t
DQ38	102	246	VSS
VSS	103	247	DQ39
DQ34	104	248	VSS
VSS	105	249	DQ35
DQ44	106	250	VSS
VSS	107	251	DQ45
DQ40	108	252	VSS
VSS	109	253	DQ41
TDQS14_t, DQS14_t, DM5_n, DBI5_n, NC	110	254	VSS
TDQS14_c, DQS14_c, NC	111	255	DQS5_c
VSS	112	256	DQS5_t
DQ46	113	257	VSS
VSS	114	258	DQ47
DQ42	115	259	VSS
VSS	116	260	DQ43
DQ52	117	261	VSS
VSS	118	262	DQ53

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9. DDR4 288 Pin UDIMM Pin Wiring As signments (Cont'd)

Front Side Pin Label	Pin	Pin	Back side Pin Label
VSS	48	192	CB5, NC
CB0, NC	49	193	VSS
VSS	50	194	CB1, NC
TDQS17_t, DQS17_t, DM8_n, DBI8_n, NC	51	195	VSS
TDQS17_c, DQS17_c, NC	52	196	DQS8_c
VSS	53	197	DQS8_t
CB6, NC	54	198	VSS
VSS	55	199	CB7, NC
CB2, NC	56	200	VSS
VSS	57	201	CB3, NC
RESET_n	58	202	VSS
VDD	59	203	CKE1
CKE0	60	204	VDD
VDD	61	205	RFU
ACT_n	62	206	VDD
BG0	63	207	BG1
VDD	64	208	ALERT_n
A12/BC_n	65	209	VDD
A9	66	210	A11
VDD	67	211	A7
A8	68	212	VDD
A6	69	213	A5
VDD	70	214	A4
A3	71	215	VDD
A1	72	216	A2
VDD	73	217	VDD

Front Side Pin Label	Pin	Pin	Back side Pin Label
DQ48	119	263	VSS
VSS	120	264	DQ49
TDQS15_t, DQS15_t, DM6_n, DBI6_n, NC	121	265	VSS
TDQS15_c, DQS15_c, NC	122	266	DQS6_c
VSS	123	267	DQS6_t
DQ54	124	268	VSS
VSS	125	269	DQ55
DQ50	126	270	VSS
VSS	127	271	DQ51
DQ60	128	272	VSS
VSS	129	273	DQ61
DQ56	130	274	VSS
VSS	131	275	DQ57
TDQS16_t, DQS16_t, DM7_n, DBI7_n, NC	132	276	VSS
TDQS16_c, DQS16_c, NC	133	277	DQS7_c
VSS	134	278	DQS7_t
DQ62	135	279	VSS
VSS	136	280	DQ63
DQ58	137	281	VSS
VSS	138	282	DQ59
SA0	139	283	VSS
SA1	140	284	VDDSPD
SCL	141	285	SDA
VPP	142	286	VPP
VPP	143	287	VPP
RFU	144	288	VPP

Note 1 Light colored text indicates functions that are not applicable for UDIMM wiring. An example is the A17 for pin 234 because UDIMMs defined by this specification will never have DIMM wiring for this pin.

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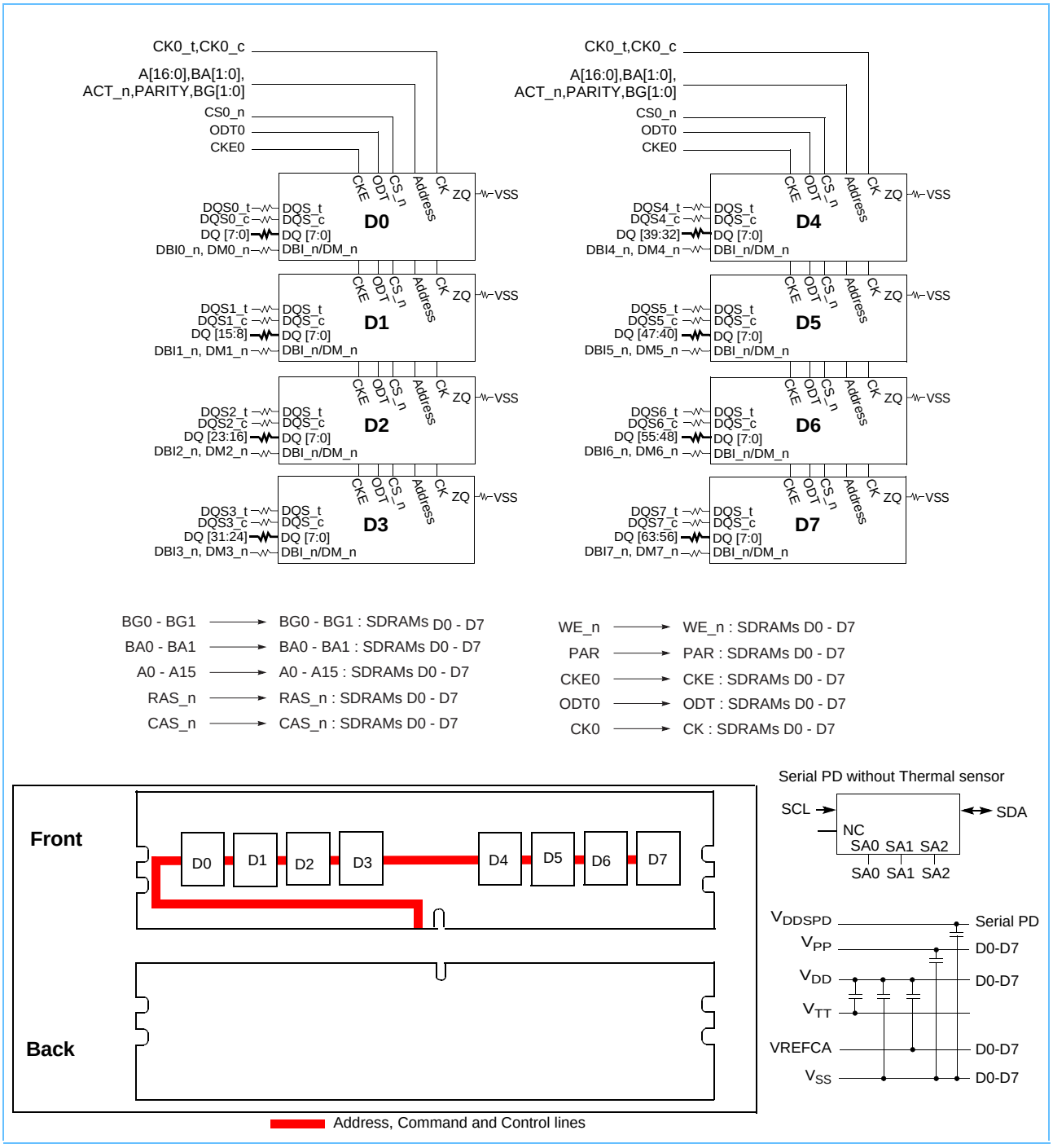
10. Functional Block Diagram

4GB, 512Mx64 Non ECC Module (Populated as 1 rank of x8 DDR4 SDRAMs)



Note 1 CK1_t, CK1_c terminated with 75 Ω ± 5% resistor.
Note 2 Unless otherwise noted resistors are 15 Ω ± 5%.
Note 3 ZQ resistors are 240 Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.
Note 4 Event_n isn't used for SPD without TS. Option Resistor for it should be unplaced.

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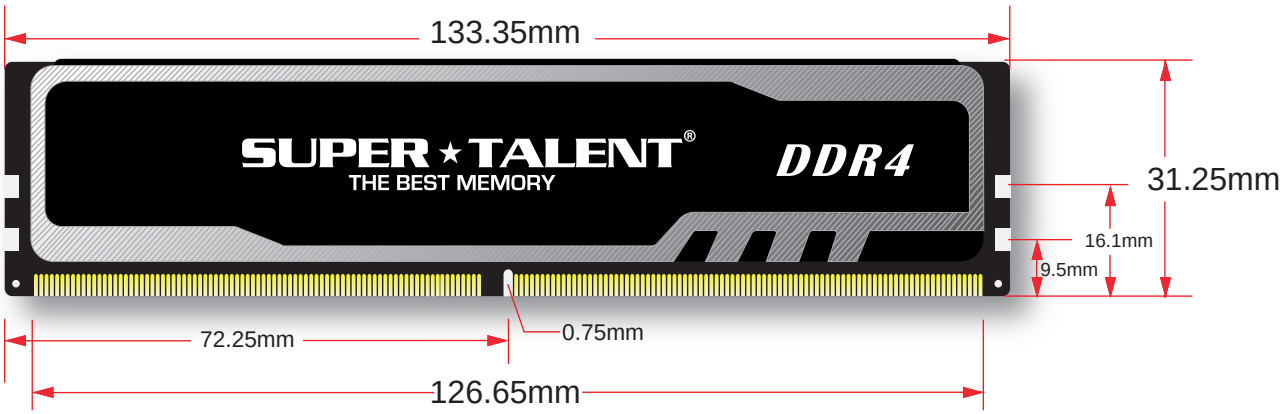
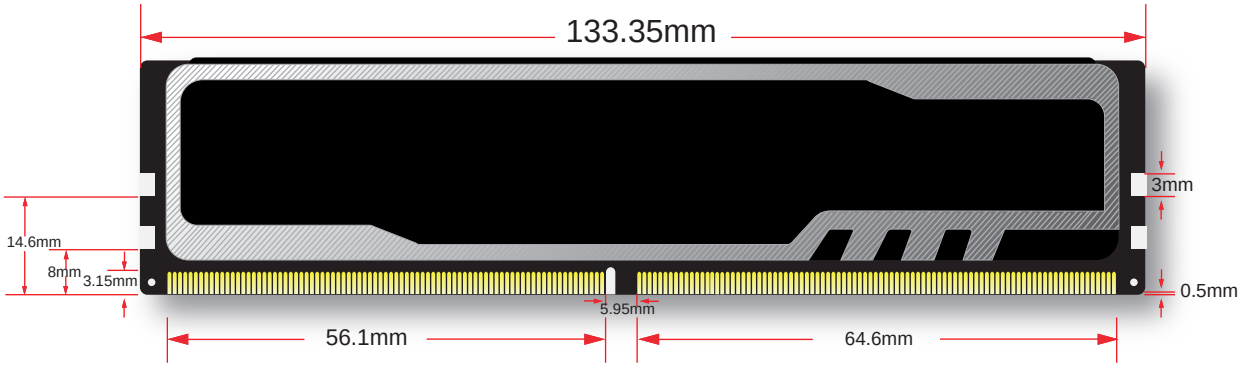
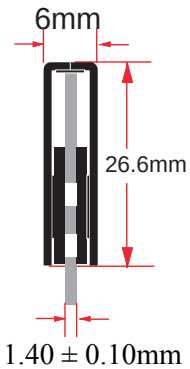
11. Physical Dimensions: (512Mbx8 Based, 4GB , 1 Rank,with heatsink)

Front



Back





Units: Millimeter
Tolerances: ± 0.15) unless otherwise specified

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