

DDR2 SDRAM FB-DIMM MODULE

512MB, 1GB, and 2GB based on 512Mbit component

4GB based on 1Gbit component

**60 FBGA with Pb-Free
(RoHS compliant)**



Revision History

Revision 1.0 (March, 2007)
-Initial Release

1. Features

- V_{DD} : +1.8V ± 0.1V, V_{DDQ} : +1.8V ± 0.1V for DDR2 SDRAM
- V_{CC} : +1.5V ± 0.1V, for Advanced Memory Buffer (AMB)
- V_{DDSPD} : +1.7V to +3.6V for SPD EEPROM
- 240-pin DDR2 FBDIMM with ECC to detect and report channel errors to the host memory controller
- High-speed differential Point-to-point serial, dual-simplex bit lanes: 10-pair southbound (to FBDIMM) and 14-pair northbound (from FBDIMM)
- 3.2 Gb/s for DDR2-533 and 4.0 Gb/s for DDR2-667
- Transmitter de-emphasis to reduce Inter Signal Interference (ISI)
- Northbound and southbound single lane fail over and channel error detection
- Support for up to 8 FB-DIMMs per channel
- SMBus interface to AMB for configuration register access; supporting-band and out-of-band command access
- Test features supported include:
 - Integrated thermal sensor and status indicator
 - Supports MBIST, IBIST and Virtual Host mode
 - Transparent mode and direct access mode for DRAM testing
- Burst Length: 4, 8 Sequential or Interleave
- Banks per SDRAM: 4 or 8
- Over-temperature detection and alert
- Serial presence detect with serial E²PROM
- SSTL_18 Interface with DDR2 SDRAM
- AMB in 655 ball FCBGA RoHS compliant package
- Pb-Free (RoHS compliant) product

2. Product Description

DIMM	DRAM	DRAM Clock	Single DIMM Bandwidth	Channel Clock	Channel Transfer Rate
PC2-4200	DDR2-533	266 MHz	4266 MB/s	133 MHz	3.2 GT/s
PC2-5300	DDR2-667	333 MHz	5333 MB/s	166 MHz	4.0 GT/s

3. FB-DIMM Ordering Information

Part Number	Density	Module Organization	Component composition	Component Package	Module rank	Description
S12TF8CJx	512MB	64Mx72	64Mx8*9	FBGA	1	PC2-4200F-444
S12TF8CMx	512MB	64Mx72	64Mx8*9	FBGA	1	PC2-5300F-555
S1GTF8AJx	1GB	128Mx72	64Mx8*18	FBGA	2	PC2-4200F-444
S1GTF8AMx	1GB	128Mx72	64Mx8*18	FBGA	2	PC2-5300F-555
S2GTF4EJx	2GB	256Mx72	128Mx4*36	FBGA	2	PC2-4200F-444
S2GTF4EMx	2GB	256Mx72	128Mx4*36	FBGA	2	PC2-5300F-555
S4GTF4FJx	4GB	512Mx72	256Mx4*36	FBGA	2	PC2-4200F-444
S4GTF4FMx	4GB	512Mx72	256Mx4*36	FBGA	2	PC2-5300F-555

Note: Last Character x of the Part Number stand for DRAM vendor

4. Product Family Attributes

DIMM organization	x72 ECC
DIMM dimensions (nominal)	5.25" x 1.195"
Pin count	240
DDR2 SDRAMs supported	512Mb
Module Capacity	64MB x72, 128MBx72, 256MBx72
Serial PD	Consistent with JC 45
Voltage options	1.8 volt (VDD/VDDQ)
Buffer Interface	High-speed Differential Point-to-point Link at 1.5 volt
DRAM Interface	SSTL_18

The reference designs for the DIMM PCBs are called the “raw cards”, abbreviated R/C. After the designs have been verified in working systems, the JEDEC JC-45 committee will post registrations of these R/C designs to the JEDEC web site for use by the industry at large.

5. Product Family Raw Card Types

Raw Card	DRAM Data Width	# of Ranks	# of DRAMs	Z-axis	Width x Height (mm)
A	x8	1	9	Planar	133.35 x 30.35
B	x8	2	18	Planar	133.35 x 30.35
E	x4	2	36	Planar	133.35 x 30.35

6. FB-DIMM Connector Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V _{DD}	121	V _{DD}	31	PN3	151	SN3	61	PN9#	181	SN9#	91	PS9#	211	SS9#
2	V _{DD}	122	V _{DD}	32	PN3#	152	SN3#	62	V _{SS}	182	V _{SS}	92	V _{SS}	212	V _{SS}
3	V _{DD}	123	V _{DD}	33	V _{SS}	153	V _{SS}	63	PN10	183	SN10	93	PS5	213	SS5
4	V _{SS}	124	V _{SS}	34	PN4	154	SN4	64	PN10#	184	SN10#	94	PS5#	214	SS5#
5	V _{DD}	125	V _{DD}	35	PN4#	155	SN4#	65	V _{SS}	185	V _{SS}	95	V _{SS}	215	V _{SS}
6	V _{DD}	126	V _{DD}	36	V _{SS}	156	V _{SS}	66	PN11	186	SN11	96	PS6	216	SS6
7	V _{DD}	127	V _{DD}	37	PN5	157	SN5	67	PN11#	187	SN11#	97	PS6#	217	SS6#
8	V _{SS}	128	V _{SS}	38	PN5#	158	SN5#	68	V _{SS}	188	V _{SS}	98	V _{SS}	218	V _{SS}
9	V _{CC}	129	V _{CC}	39	V _{SS}	159	V _{SS}	KEY				99	PS7	219	SS7
10	V _{CC}	130	V _{CC}	40	PN13	160	SN13	69	V _{SS}	189	V _{SS}	100	PS7#	220	SS7#
11	V _{SS}	131	V _{SS}	41	PN13#	161	SN13#	70	PS0	190	SS0	101	V _{SS}	221	V _{SS}
12	V _{CC}	132	V _{CC}	42	V _{SS}	162	V _{SS}	71	PS0#	191	SS0#	102	PS8	222	SS8
13	V _{CC}	133	V _{CC}	43	V _{SS}	163	V _{SS}	72	V _{SS}	192	V _{SS}	103	PS8#	223	SS8#
14	V _{SS}	134	V _{SS}	44	RFU*	164	RFU*	73	PS1	193	SS1	104	V _{SS}	224	V _{SS}
15	V _{TT}	135	V _{TT}	45	RFU*	165	RFU*	74	PS1#	194	SS1#	105	RFU**	225	RFU**
16	VID1	136	VID0	46	V _{SS}	166	V _{SS}	75	V _{SS}	195	V _{SS}	106	RFU**	226	RFU**
17	RESET#	137	DNU/M_Test	47	V _{SS}	167	V _{SS}	76	PS2	196	SS2	107	V _{SS}	227	V _{SS}
18	V _{SS}	138	V _{SS}	48	PN12	168	SN12	77	PS2#	197	SS2#	108	V _{DD}	228	SCK
19	RFU**	139	RFU**	49	PN12#	169	SN12#	78	V _{SS}	198	V _{SS}	109	V _{DD}	229	SCK#
20	RFU**	140	RFU**	50	V _{SS}	170	V _{SS}	79	PS3	199	SS3	110	V _{SS}	230	V _{SS}
21	V _{SS}	141	V _{SS}	51	PN6	171	SN6	80	PS3#	200	SS3#	111	V _{DD}	231	V _{DD}
22	PN0	142	SN0	52	PN6#	172	SN6#	81	V _{SS}	201	V _{SS}	112	V _{DD}	232	V _{DD}
23	PN0#	143	SN0#	53	V _{SS}	173	V _{SS}	82	PS4	202	SS4	113	V _{DD}	233	V _{DD}
24	V _{SS}	144	V _{SS}	54	PN7	174	SN7	83	PS4#	203	SS4#	114	V _{SS}	234	V _{SS}
25	PN1	145	SN1	55	PN7#	175	SN7#	84	V _{SS}	204	V _{SS}	115	V _{DD}	235	V _{DD}
26	PN1#	146	SN1#	56	V _{SS}	176	V _{SS}	85	V _{SS}	205	V _{SS}	116	V _{DD}	236	V _{DD}
27	V _{SS}	147	V _{SS}	57	PN8	177	SN8	86	RFU*	206	RFU*	117	V _{TT}	237	V _{TT}
28	PN2	148	SN2	58	PN8#	178	SN8#	87	RFU*	207	RFU*	118	SA2	238	V _{DDSPD}
29	PN2#	149	SN2#	59	V _{SS}	179	V _{SS}	88	V _{SS}	208	V _{SS}	119	SDA	239	SA0
30	V _{SS}	150	V _{SS}	60	PN9	180	SN9	89	V _{SS}	209	V _{SS}	120	SCL	240	SA1
								90	PS9	210	SS9				

Notes:

RFU = Reserved Future Use.

* These pins are reserved for forwarded clocks to be used in future module implementations

** These pins are reserved for future architecture flexibility

The following signals are CRC bits and thus appear out of the normal sequence:

PN12/PN12#, SN12/SN12#, PN13/PN13#, SN13/SN13#, PS9/PS9#, SS9/SS9#

7. FBDIMM Connector Pin description

Pin Name	Description	Pin Name	Description
PN[13:0]	Primary Northbound Data, positive lines	SCL	Serial Presence Detect (SPD) Clock Input
PN[13:0]#	Primary Northbound Data, negative lines	SDA	SPD Data Input / Output
PS[9:0]	Primary Southbound Data, positive lines	SA[2:0]	SPD Address Inputs, also used to select the DIMM number in the AMB
PS[9:0]#	Primary Southbound Data, negative lines	VID1	Voltage ID1 for V _{cc} Value: OPEN = 1.5V, GND = 1.2V
SN[13:0]	Secondary Northbound Data, positive lines	VID0	Voltage ID0 for V _{dd} Value: OPEN = 1.8V, GND = 1.5V
SN[13:0]#	Secondary Northbound Data, negative lines	RESET	AMB reset signal
SS[9:0]	Secondary Southbound Data, positive lines	V _{CC}	AMB Core Power and Channel Interface Power (1.5 V)
SS[9:0]#	Secondary Southbound Data, negative lines	V _{DD}	DRAM Power and AMB DRAM I/O Power (1.8 V)
SCK	System clock Input, positive line ¹	V _{TT}	DRAM Address/Command/Clock Termination Power (V _{DD} /2)
SCK#	System clock Input, negative line ¹	V _{DDSPD}	SPD Power
RFU	Reserved for Future Use ²	V _{SS}	Ground
DNU/M _{Test}	The DNU/M _{Test} pin provides an external connection on R/Cs A-D for testing the margin of V _{REF} which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and if it does, will be included in this specification at that time.		

Notes:

¹: System Clock Signals SCK and SCK# switch at one half the DRAM CK/CK# frequency

²: Eight pins reserved for forwarded clocks, eight pins reserved for future architecture flexibility

8. Address Configuration

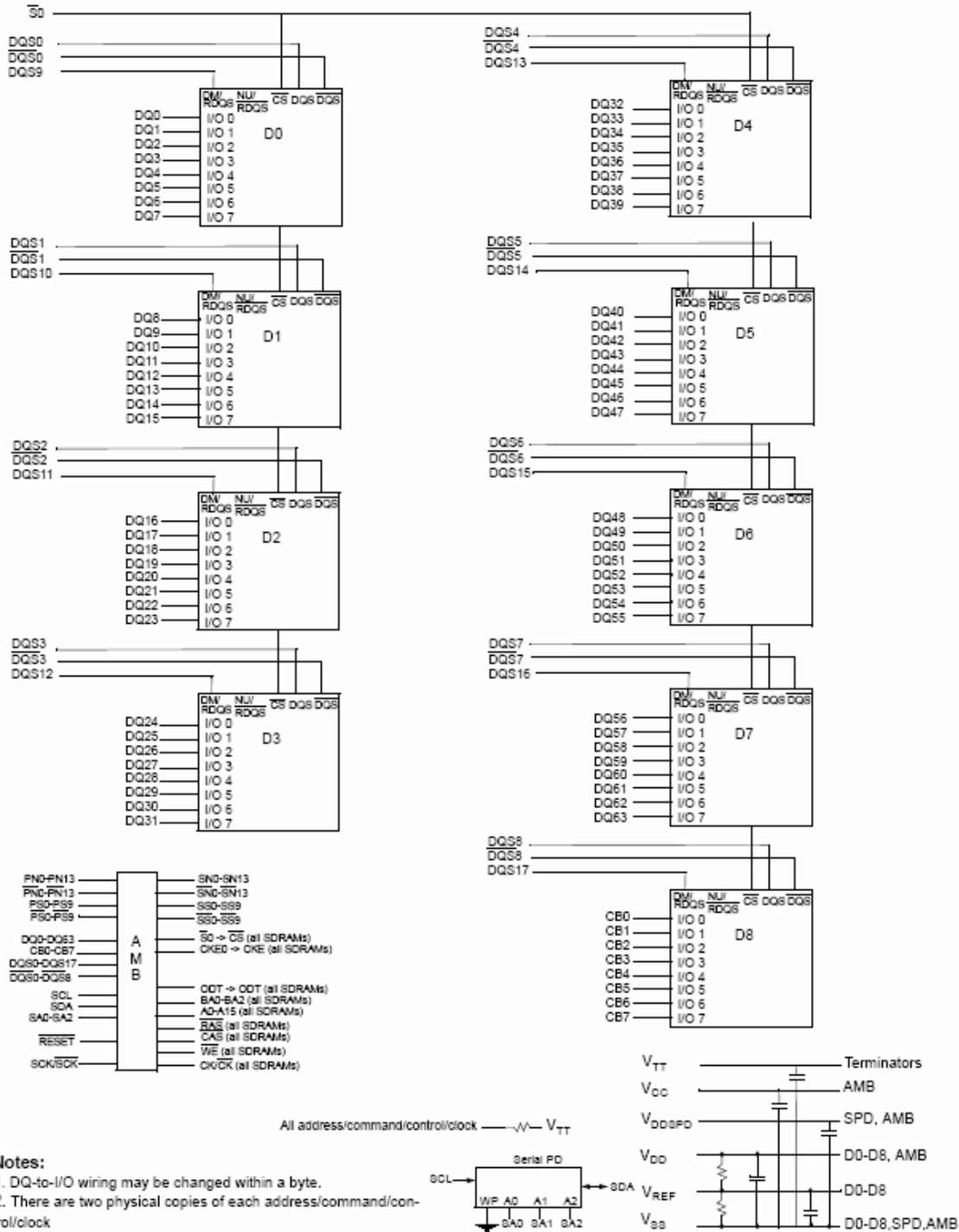
Organization	Row Address	Column Address	Bank Address	Auto Precharge
64Mx8(512Mb) base	A0-A13	A0-A9	BA0-BA1	A10
128Mx4 (512Mb) base	A0-A13	A0-A9	BA0-BA1	A10
128Mx4 (512Mb) base	A0-A13	A0-A9	BA0-BA2	A10

9. Performance Range

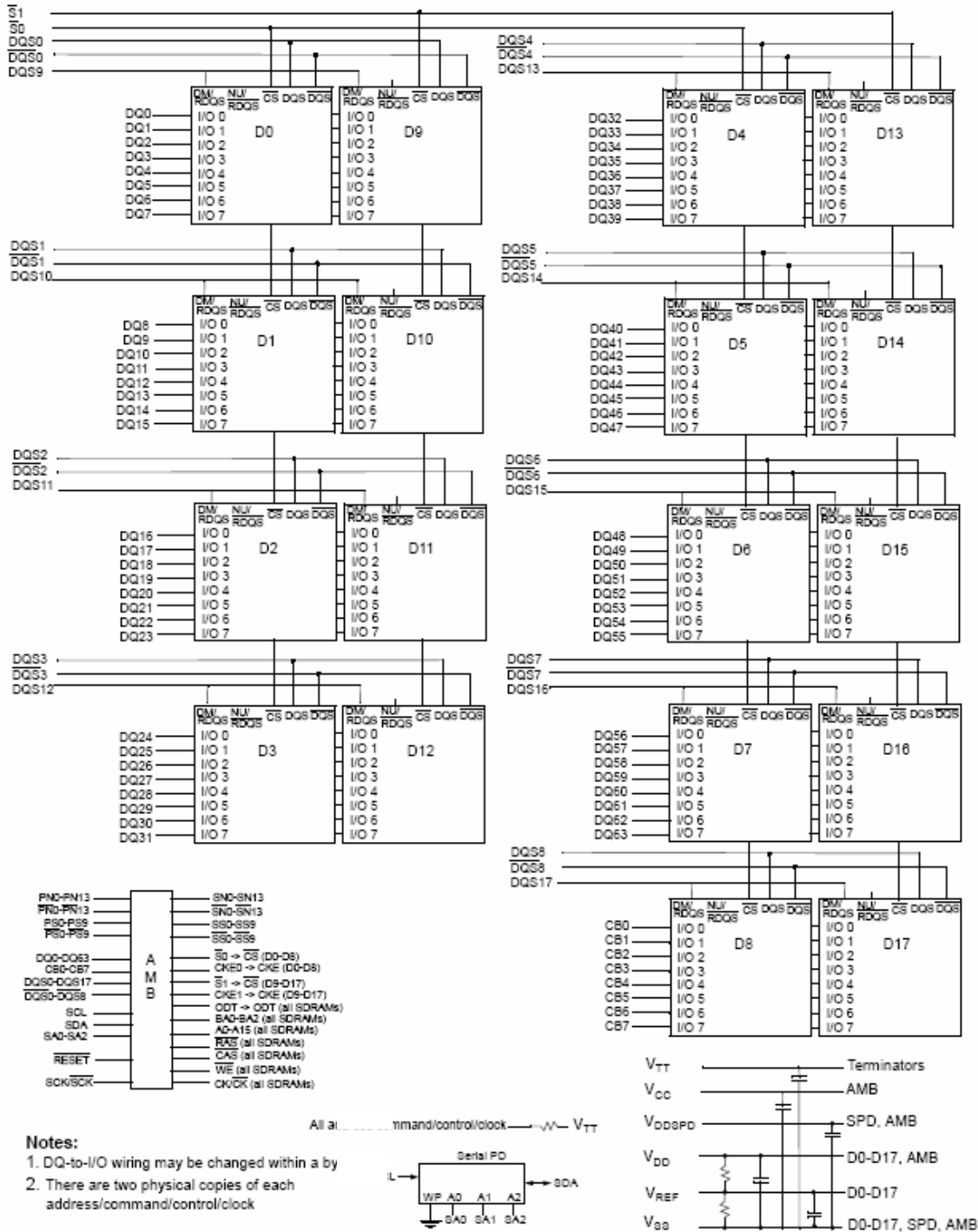
	DDR2-533@CL=4	DDR2-667@CL=5
Speed @CL4	266MHz	266Mhz
Speed @CL5	-	333Mhz
CL-t _{RCD} -t _{RP}	4-4-4	5-5-5

10. Block Diagram:

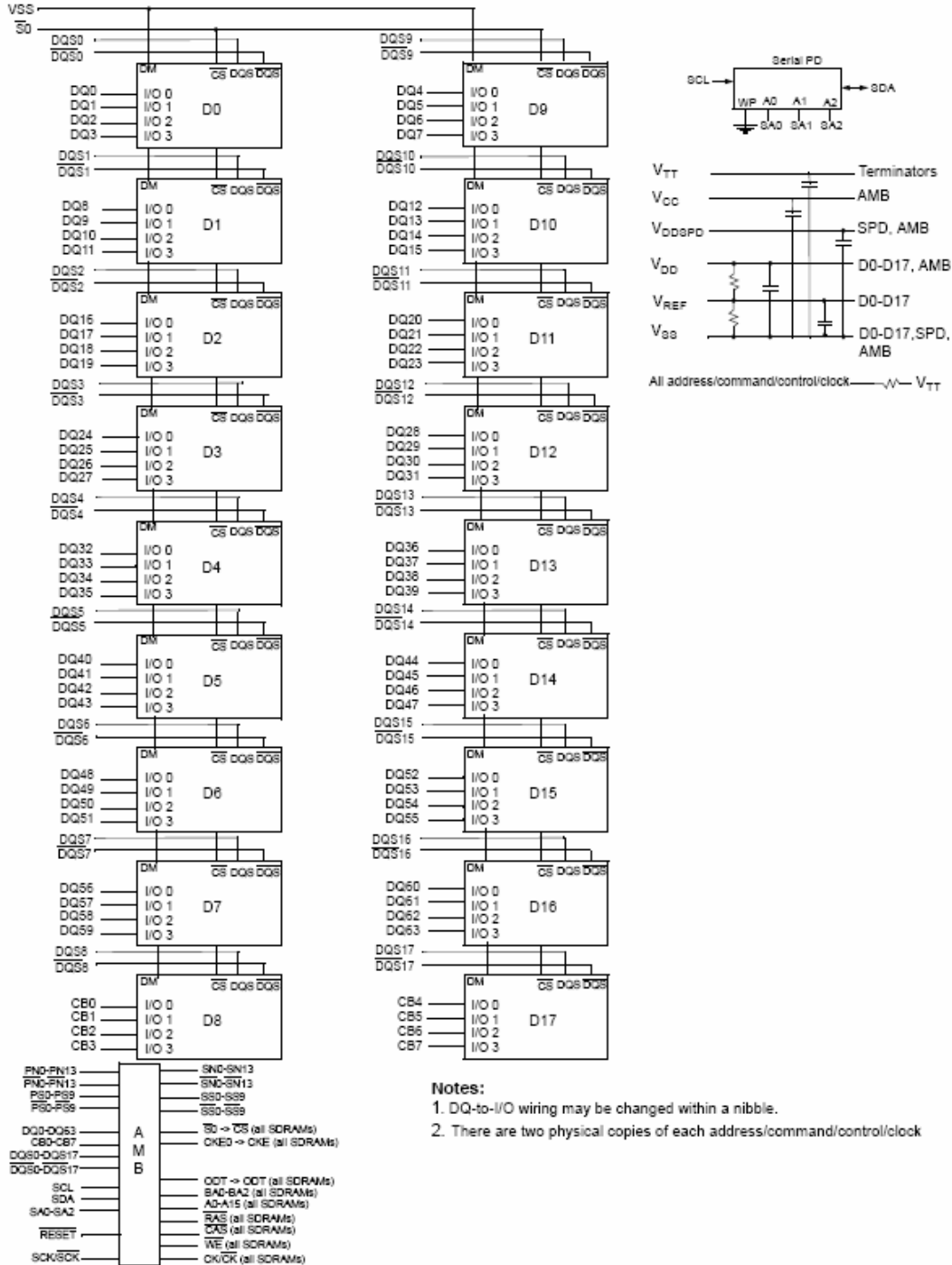
10.1 x72 ECC DIMM, populated as 1 rank of x8 DDR2 SDRAM



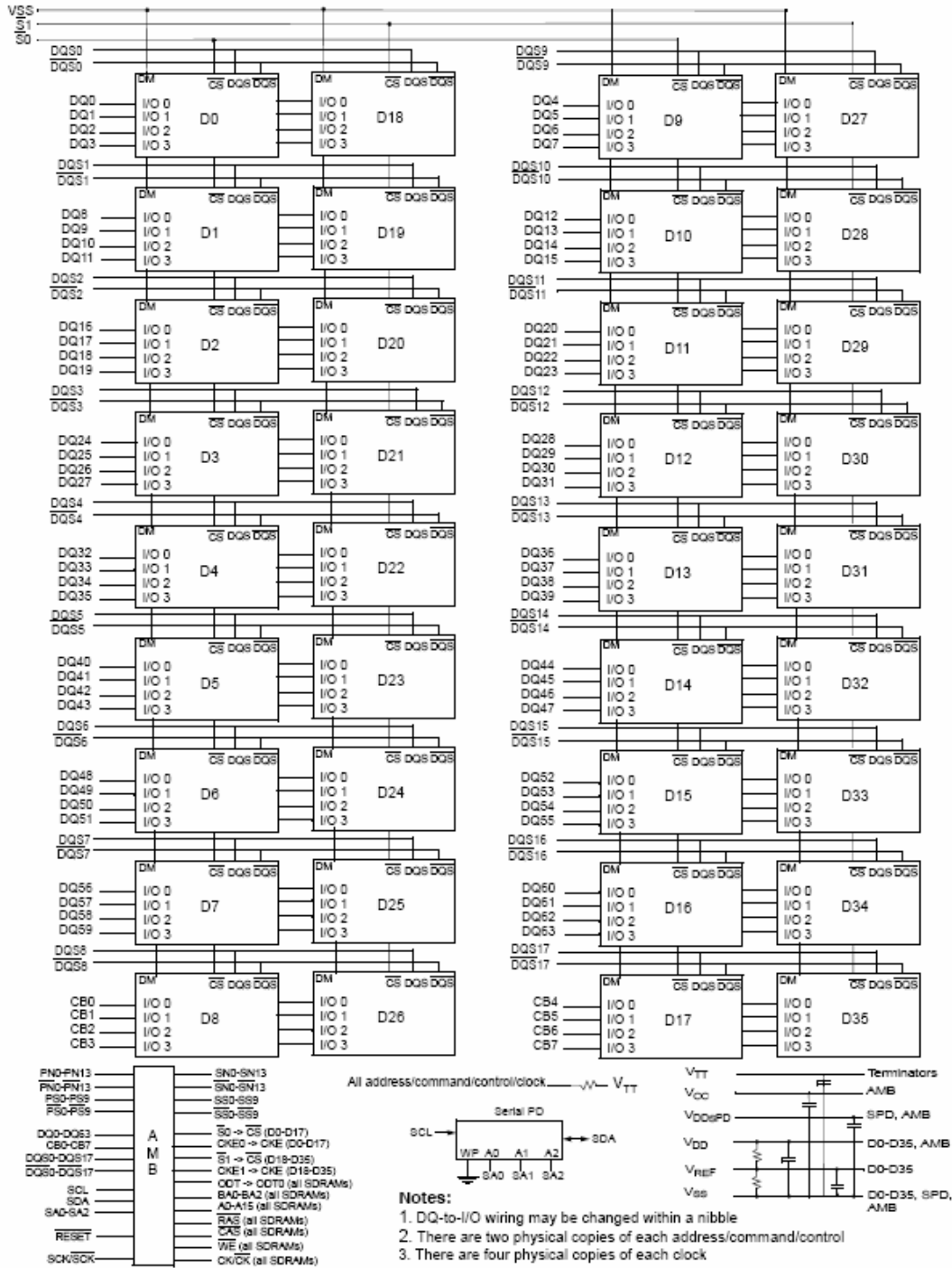
10.2 x72 ECC DIMM, populated as 2 ranks of x8 DDR2 SDRAM



10.3 x72 ECC DIMM, populated as 1rank of x4 DDR2 SDRAM



10.4 x72 ECC DIMM, populated as 2 ranks of x4 DDR2 SDRAM



11. Absolute Maximum DC Rating

Symbol	Parameter	Rating	Units
V _{DD}	Voltage on V _{DD} pin relative to V _{SS}	-0.5V ~ 2.3V	V
V _{CC}	Voltage on V _{CC} pin relative to V _{SS}	-0.3V ~ 1.75V	V
V _{IN,OUT}	Voltage on any pin relative to V _{SS}	-0.3V ~ 1.75V	V
V _{TT}	Voltage on V _{TT} pin relative to V _{SS}	-0.5V ~ 2.3V	V
T _{STG}	Storage Temperature	-55 ~ +100	°C
T _{CASE,DRAM}	DDR2 SDRAM device operating temperature (Ambient)	-0 ~ +85	°C
T _{CASE,AMB}	AMB device operating temperature (Ambient)	-0 ~ +85	°C

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

12. DC Voltage and Operating Conditions

Parameter	Symbol	Min.	Nom.	Max.	Units	Notes
AMB Supply Voltage	V _{CC}	1.425	1.5	1.59	V	
DDR2 SDRAM Supply Voltage	V _{DD}	1.7	1.8	1.9	V	
Termination Voltage	V _{TT}	0.48 x V _{DD}	0.50 x V _{DD}	0.52 x V _{DD}	V	
EEPROM Supply Voltage	V _{DDSPD}	3.0	3.3	3.6	V	
DC Input logic High (SPD)	V _{IH} (DC)	2.1	--	V _{DDSPD}	V	1
DC Input logic Low (SPD)	V _{IL} (DC)	--	--	0.8	V	1
DC Input logic High (RESET)	V _{IH} (DC)	1.0	--	--	V	2
DC Input logic Low (RESET)	V _{IL} (DC)	--	--	0.5	V	1
Leakage Current (RESET)	I _L	-90	--	90	μA	2
Leakage Current (link)	I _L	-5	--	5	μA	

- Note:
1. Applies for SMB and SPD signals.
 2. Applies for AMB CMOS signal RESET#

13. Environment Parameters

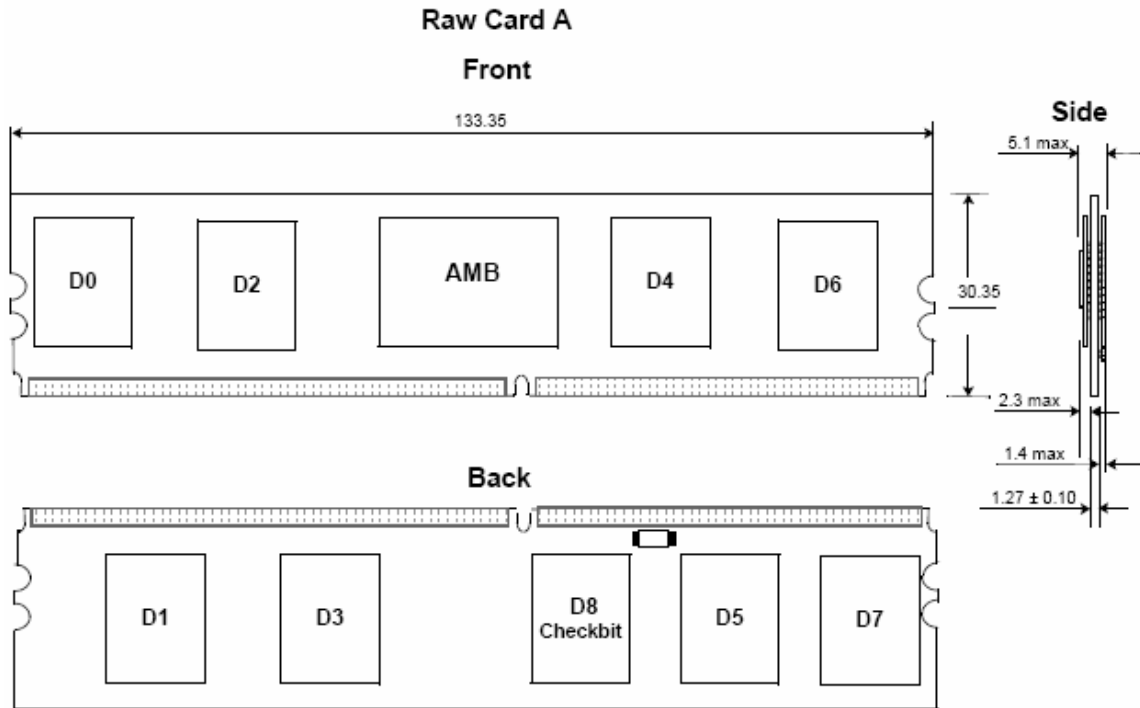
Symbol	Parameter	Rating	Units	Notes
T _{OPR}	Operating Temperature	See Note	°C	1
H _{OPR}	Operating humidity (relative)	10 to 90	%	2
T _{STG}	Storage temperature	-50 to +100	°C	2
H _{STG}	Storage humidity (without condensation)	5 to 95	%	2
P _{BAR}	Barometric pressure (operating)	3050	m	2
P _{BAR}	Barometric pressure (storage)	15240	m	2

- Notes:
1. The designer must meet the case temperature specifications for individual module components.
 2. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

14. Mechanical Dimension

14.1 Raw Card A

64Mx72 (1 rank x8 Base component)

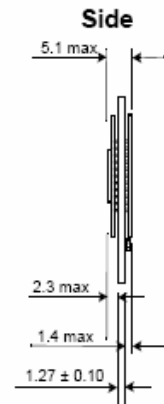
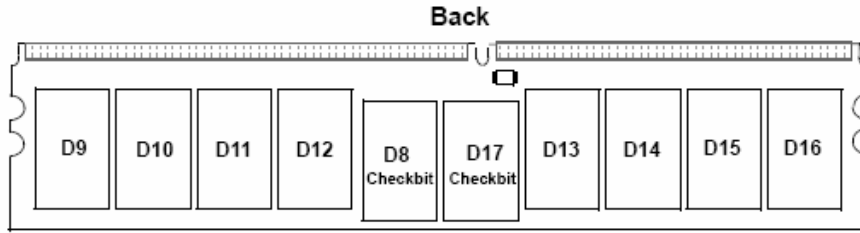
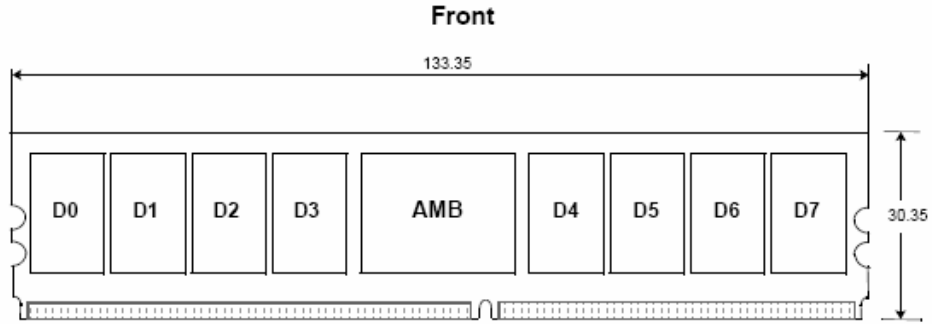


Note 1: All dimensions (in mm) are typical unless otherwise stated.

Note 2: Support for 16.5 mm wide by 21.9 mm tall DRAM footprint.

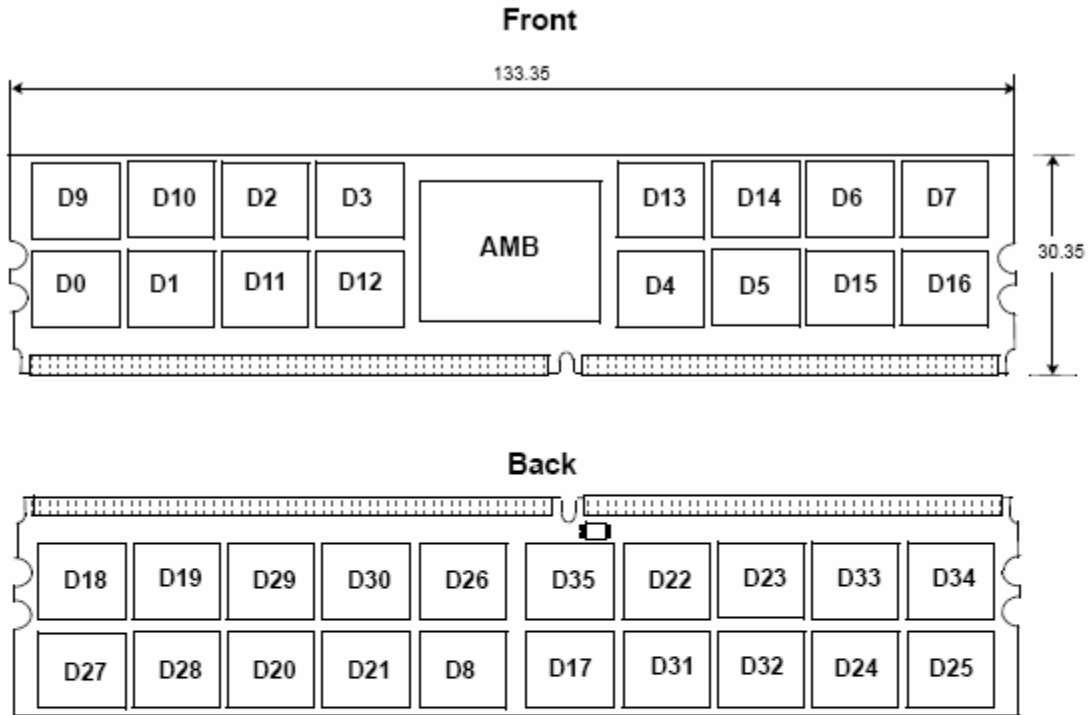
Note 3: Thickness is stated w/o Heat Spreader.

14.2 Mechanical Dimension: Raw Card B
128Mx72(2rank x8 Base component)



Note 1: All dimensions (in mm) are typical unless otherwise stated.
Note 2: Thickness is stated w/o Heat Spreader.

14.3 Mechanical Dimension: Raw card E
256Mx72/512Mx72 (2 rank x4 Base component)



Side²



- Note 1:** All dimensions (in mm) are typical unless otherwise stated.
- Note 2:** Heat Spreader Assembly not shown, refer to MO-256 for thickness dimensions.

14.4 Package outline with Full Heat Spreader

