

1.3" IDE Solid State Drive

General Description

The IDE Flash Drive FHD8/16/32GC13M series is an IDE interface solid state disk (SSD) drive that features a flash disk controller chip and NAND type flash memory devices. This 1.3 inch form factor SSD series is available in 8GB, 16GB, and 32GB capacities. The drive uses a 5-volt power supply and supports up to PIO Mode 6, MDMA Mode 4, and UDMA Mode 5. This IDE SSD Drive is geared specifically to military and industrial markets for use in such products as ATM, factory automation machines, POS terminals, measuring products, ticket vending machines, parking systems and other industrial products that require high tolerance to environmental conditions.

Features

- Capacity: 8GB to 32GB
- Form factor: 1.3 inch type (HDD compatible)
- IDE interface: Up to PIO Mode 6,
 - MDMA Mode 4,
 - UDMA Mode 5
- Power supply: Vcc=5.0V +/-5%
- Operating temperature: Commercial: 0C to +70C
- Performance:
 - Sequential Read Rate: 28MB/sec (min)
 - Sequential Write Rate: 26MB/sec (min)
 - Access Time: 0.1ms
- Shock: 1500G (operating)
- Vibration: 16G (operating)

Specifications

- Compatibility: Full IDE hard disk compatible
- OS Support: All
- Package: Complete metal housing
- Reliability:
 - MTBF: >1,000,000 hours
 - Data reliability: Built-in EDC/ECC function
 - Patent pending Wear-leveling algorithms
- Endurance:
 - Read: Unlimited
 - Write/Erase: >140 years @ 50GB write-erase /day



Designed and Manufactured in USA

Ordering Information

Capacity	Model No.
8GB	FHD8GC13M
16GB	FHD16GC13M
32GB	FHD32GC13M

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
Vcc	Power Supply Voltage	-0.3 to 6.5	V
V _{IH}	Input Voltage	-0.5 to Vcc+0.5	V
T _{STG}	Storage Temperature	-65 to 150	°C
T _{OPR}	Operating Temperature	Commercial	-0 to 70
		Industrial	-40 to 85

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
Vcc	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	High Level Input Voltage	2.0	-	-	V
V _{IL}	Low Level Input Voltage	-	-	0.8	V

DC CHARACTERISTICS (T_a = -40°C to 85°C, Vcc = 5V ± 10%)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
I _{CCO}	Operating Current	-	40	-	µA
I _{CCS}	Sleep Mode Current	-	-	1.2	µA
V _{OH}	High Level Output Voltage	Vcc-0.8	-	-	V
V _{OL}	Low Level Output Voltage	-	-	0.4	V

System Requirements

- In order to install the 1.3" Flash Drive in your system, ensure that you have the following items:
- System mounting hardware
 - 44 pin ribbon IDE cable

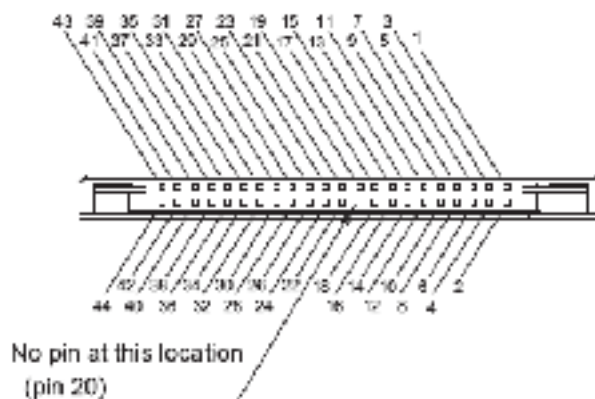


Figure 1: 1.3" Flash Drive Pin Configuration

Pin Assignment 44 Pin IDE Flash Drive			
PIN	SYMBOL	PIN	SYMBOL
1	WRSTP	2	GM5
3	HD7	4	HD8
5	HLR	6	HLJ
7	HDE	8	HD10
9	HD4	10	HD11
11	HD9	12	HD12
13	HD2	14	HD13
15	HL7	16	HL14
17	HDC	18	HD15
19	GND	20	Ksv
21	DMARQ	22	GND
23	LOW	24	GND
25	KCR	26	GND
27	MAF	28	CSBL
29	DMACK	30	GND
31	HC	32	IOE11
33	IA1	34	PDAG
35	IA0	36	HA2
37	CSH	38	ICS1
39	DMASP	40	GND
41	Vcc	42	Vcc
43	GND	44	NC

Revision History

Aug 17, 2007 Rev-A Preliminary Product Specification Released
March 21, 2008 Rev-B Updated Photo

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CONFIGURATION DESCRIPTIONS

Signal Name	Dir	Pin	Description
HA[2:0]	I	36, 33, 35	A2-A0 are used to select the one of the eight registers in the Task File
/CS[1:0]	I	38, 37	/CS0 is the chip select for the Task File registers while /CS1 is used to select the Alternative Status Register and the Device Control Register
CSEL	I	28	This internally pulled-up signal is used to configure this device as a Master or a Slave, if J_CSEL_-EN is grounded by a jumper from B to D. When the pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
HD[15:0]	I/O	18, 16, 14, 12, 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17	All the Task File operations occur in byte mode on the low order bus HD[7:0] while all data transfers are 16 bit using HD[15:0].
/DASP	I/O	39	This input/output is the Disk Active/ Slave Present signal in the Master/Slave handshake protocol.
DMARQ	O	21	DMA transfer request
/DMACK	I	29	DMA request knowledge
/IOW:STOP	I	23	The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the Drive controller registers when the Drive is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge). During Ultra DMA, this is the stop signal.
/IOR: HDMARDY/ HSTROBE	I	25	This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the Drive. Ultra DMA control signal used to extend host transfer cycles.
IRQ	O	31	Signal used to interrupt host when service is requested.
/IOIS16	O	32	This output signal is asserted low when this device is expecting a word data transfer cycle.
IORDY: DDMARDY/ DSTROBE	O	27	This output signal may be used as IORDY. Ultra DMA control signal used to extend host transfer cycles.
/PDIAG	I/O	34	This input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
/RESET	I	1	This input pin is the active low hardware reset from the host.
GND	--	2, 19, 22, 24, 26, 30, 40, 43	Ground
Key	--	20	This pin is keyed so that the drive can only be connected with the cable pin 1 to drive pin 1.
N/C	--	44	No connect
Vcc	--	42, 41	+5V

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Mechanical Specification

