DDR SDRAM UNBUFFERED DIMM

D21PB12A – 512MB with heat spreader
D21PB1GH – 1GB with heat spreader

For the latest data sheet, please visit the Super Talent Electronics web site: www.supertalentmemory.com

Features:

- 184-pin, dual in-line memory module (DIMM)
- Fast data transfer rates: PC2100
- Utilizes 266 MT/s DDR SDRAM components
- 512MB (64 Meg x 64) and 1GB (128 Meg x 64)
- VDD = VDDQ = +2.5V
- VDDSPD = +2.3V to +3.6V
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; centeraligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted / received with data—i.e., source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Four internal device banks for concurrent operation
- Programmable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 7.8125µs (512MB, 1GB) maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Programmable READ CAS latency
- Gold edge contacts

Figure 1: 184-Pin DIMM – under heat spreader

Table 1: Address Table

	512MB	1GB
Refresh Count	8K	8K
Row Addressing	8K (A0–A12)	8K (A0–A12)
Device Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)
Device Configuration	256Mb (32 Meg x 8)	512Mb (64 Meg x 8)
Column Addressing	1K (A0–A9)	2K (A0–A9, A11)
Module Rank Addressing	2 (S0#, S1#)	2 (S0#, S1#)

Table 2: Pin Assignment (184-Pin DIMM Front)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VREF	24	DQ17	47	DNU	70	VDD
2	DQ0	25	DQS2	48	A0	71	NC
3	VSS	26	VSS	49	DNU	72	DQ48
4	DQ1	27	A9	50	VSS	73	DQ49
5	DQS0	28	DQ18	51	DNU	74	VSS
6	DQ2	29	A7	52	BA1	75	CK2#
7	VDD	30	VDDQ	53	DQ32	76	CK2
8	DQ3	31	DQ19	54	VDDQ	77	VDDQ
9	NC	32	A5	55	DQ33	78	DQS6
10	NC	33	DQ24	56	DQS4	79	DQ50
11	VSS	34	VSS	57	DQ34	80	DQ51
12	DQ8	35	DQ25	58	VSS	81	VSS
13	DQ9	36	DQS3	59	BA0	82	NC
14	DQS1	37	A4	60	DQ35	83	DQ56
15	VDDQ	38	VDD	61	DQ40	84	DQ57
16	CK1	39	DQ26	62	VDDQ	85	VDD
17	CK1#	40	DQ27	63	WE#	86	DQS7
18	VSS	41	A2	64	DQ41	87	DQ58
19	DQ10	42	VSS	65	CAS#	88	DQ59
20	DQ11	43	A1	66	VSS	89	VSS
21	CKE0	44	DNU	67	DQS5	90	NC
22	VDDQ	45	DNU	68	DQ42	91	SDA
23	DQ16	46	VDD	69	DQ43	92	SCL

Table 3: Pin Assignment (184-Pin DIMM Back)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
93	VSS	116	VSS	139	VSS	162	DQ47
94	DQ4	117	DQ21	140	DNU	163	NC
95	DQ5	118	A11	141	A10	164	VDDQ
96	VDDQ	119	DM2	142	DNU	165	DQ52
97	DM0	120	VDD	143	VDDQ	166	DQ53
98	DQ6	121	DQ22	144	DNU	167[2]	NC/A13
99	DQ7	122	A8	145	VSS	168	VDD
100	VSS	123	DQ23	146	DQ36	169	DM6
101	NC	124	VSS	147	DQ37	170	DQ54
102	NC	125	A6	148	VDD	171	DQ55
103	NC	126	DQ28	149	DM4	172	VDDQ
104	VDDQ	127	DQ29	150	DQ38	173	NC
105	DQ12	128	VDDQ	151	DQ39	174	DQ60
106	DQ13	129	DM3	152	VSS	175	DQ61
107	DM1	130	A3	153	DQ44	176	VSS
108	VDD	131	DQ30	154	RAS#	177	DM7
109	DQ14	132	VSS	155	DQ45	178	DQ62
110	DQ15	133	DQ31	156	VDDQ	179	DQ63
111	CKE1	134	DNU	157	S0#	180	VDDQ
112	VDDQ	135	DNU	158	S1#	181	SA0
113	NC	136	VDDQ	159	DM5	182	SA1
114	DQ20	137	CK0	160	VSS	183	SA2
115	NC/A12	138	CK0#	161	DQ46	184	VDDSPD

Notes:
1. **Pin 115 is A12**
2. **Pin 167 is No Connect (NC)**

Figure 3:
Pin Locations

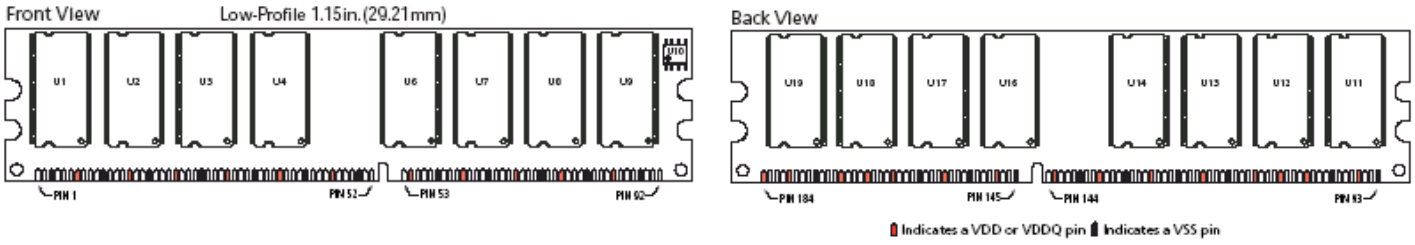


Table 4: Pin Descriptions

Pin numbers may not necessarily correlate with symbols. Refer to Pin Assignment tables on page 2 for more information.

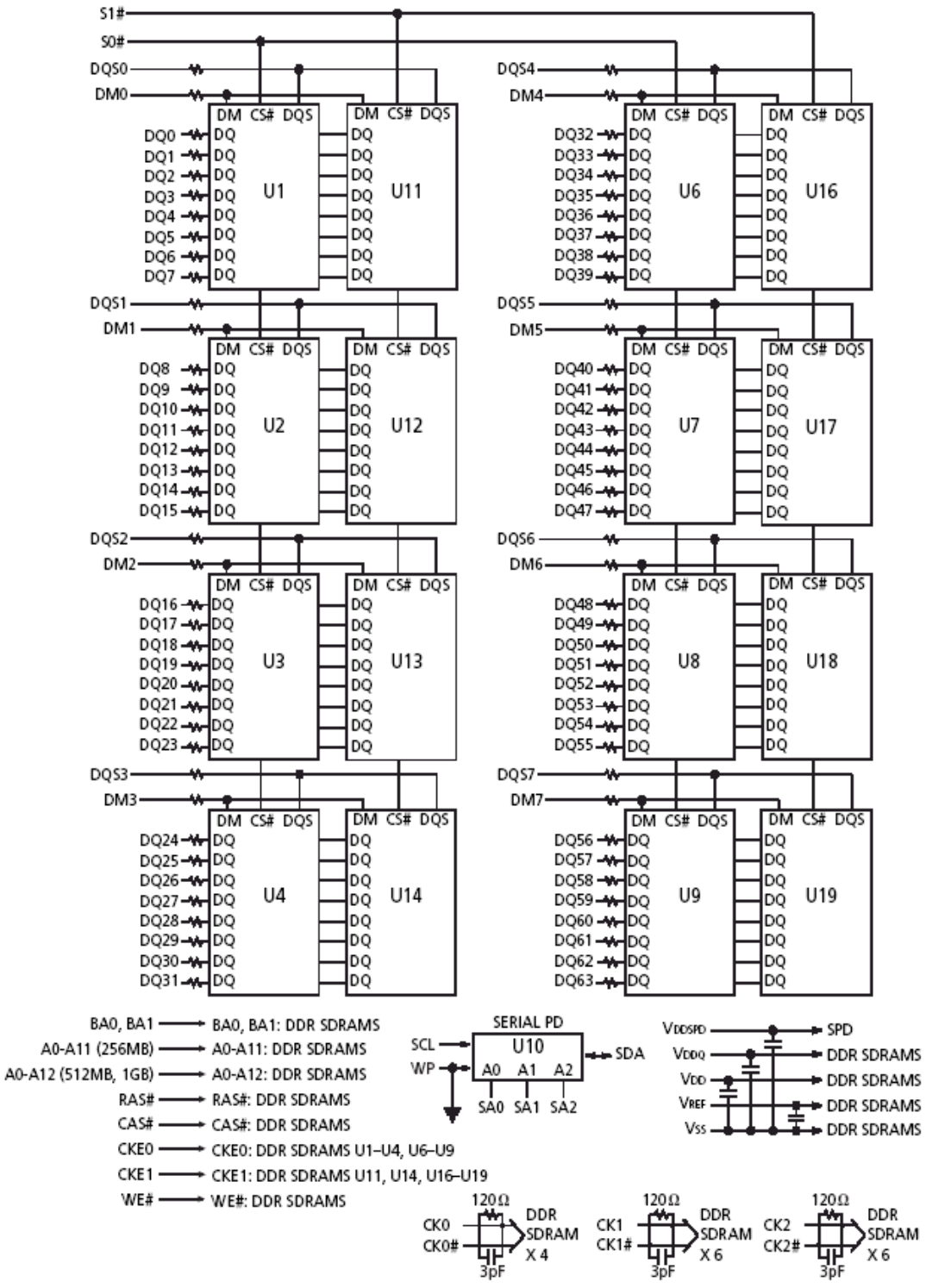
PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
63, 65, 154	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
16, 17, 75, 76, 137, 138	CK0, CK0#, CK1, CK1#, CK2, CK2#	Input	Clock: CK, CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK, and negative edge of CK#. Output data (DQs and DQS) is referenced to the crossings of CK and CK#.
21, 111	CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all device banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any device bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK# and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after VDD is applied and until CKE is first brought HIGH. After CKE is brought HIGH, it becomes an SSTL_2 input only.
157, 158	S0#, S1#	Input	Chip Selects: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
52, 59	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
27, 29, 32, 37, 41, 43, 48, 115 (512MB, 1GB, 2GB), 118, 122, 125, 130, 141, 167 (2GB)	A0–A11 (256MB) A0–A12 (512MB, 1GB) A0–A13 (2GB)	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
5, 14, 25, 36, 56, 67, 78, 86	DQS0–DQS7	Input/ Output	Data Strobe: Output with READ data, input with WRITE data. DQS is edge-aligned with READ data, centered in WRITE data. Used to capture data.
97, 107, 119, 129, 149, 159, 169, 177	DM0–DM7	Input	Data Write Mask: DM LOW allows WRITE operation. DM HIGH blocks WRITE operation. DM lines do not affect READ operation.

Table 5: Pin Descriptions (continued)

Pin numbers may not necessarily correlate with symbols. Refer to Pin Assignment tables on page 2 for more information.

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
2, 4, 6, 8, 12, 13, 19, 20, 23, 24, 28, 31, 33, 35, 39, 40, 53, 55, 57, 60, 61, 64, 68, 69, 72, 73, 79, 80, 83, 84, 87, 88, 94, 95, 98, 99, 105, 106, 109, 110, 114, 117, 121, 123, 126, 127, 131, 133, 146, 147, 150, 151, 153, 155, 161, 162, 165, 166, 170, 171, 174, 175, 178, 179	DQ0–DQ63	Input/ Output	Data I/Os: Data bus.
92	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
181,182, 183	SA0–SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
91	SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect device.
1	V_{REF}	Supply	SSTL_2 reference voltage.
15, 22, 30, 54, 62, 77, 96, 104, 112, 128, 136, 143, 156, 164, 172, 180	V_{DDQ}	Supply	DQ Power Supply: +2.5V ±0.2V.
7, 38, 46, 70, 85, 108, 120, 148, 168	V_{DD}	Supply	Power Supply: +2.5V ±0.2V.
3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 81, 89, 93, 100, 116, 124, 132, 139, 145, 152, 160, 176	V_{SS}	Supply	Ground.
184	V_{DDSPD}	Supply	Serial EEPROM positive power supply: +2.3V to +3.6V.
44, 45, 47, 49, 51, 134, 135, 140, 142, 144	DNU	—	Do Not Use: These pins are not connected on these modules, but are assigned pins on other modules in this product family.
9, 10, 71, 82, 90, 101, 102, 103, 113, 115 (256MB), 163, 167 (256MB, 512MB, 1GB), 173	NC	—	No Connect: These pins should be left unconnected.

Figure 4: Functional Block Diagram - Low Profile



Note:

1. All resistor values are 22Ω unless otherwise specified.

General Description:

The D21PB12A and D21PB1GH are high-speed CMOS, dynamic random-access, 512MB and 1GB memory modules organized in x64 configuration.

DDR SDRAM modules use internally configured quad-bank DDR SDRAM devices. DDR SDRAM modules use double data rate architecture to achieve high-speed operation. Double data rate architecture is essentially a 2n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM module effectively consists of a single 2n-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bi-directional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to DDR SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select devices bank; A0–A12 select device row for 512MB, 1GB). The address bits registered coincident with the READ or WRITE command are used to select the device bank and the starting device column location for the burst access.

DDR SDRAM modules provide for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto pre-charge function may be enabled to provide a self-timed row pre-charge that is initiated at the end of the burst access.

The pipelined, multibank architecture of DDR SDRAM modules allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

Serial Presence- Detect Operation

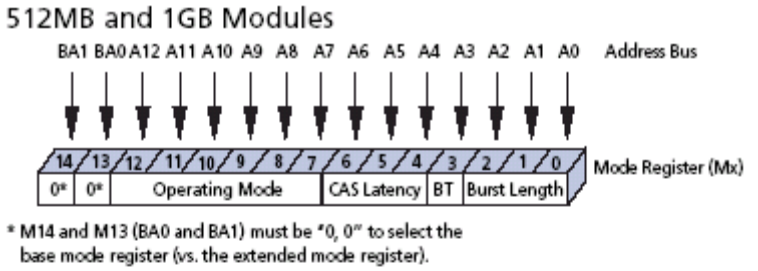
DDR SDRAM modules incorporate serial presence detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

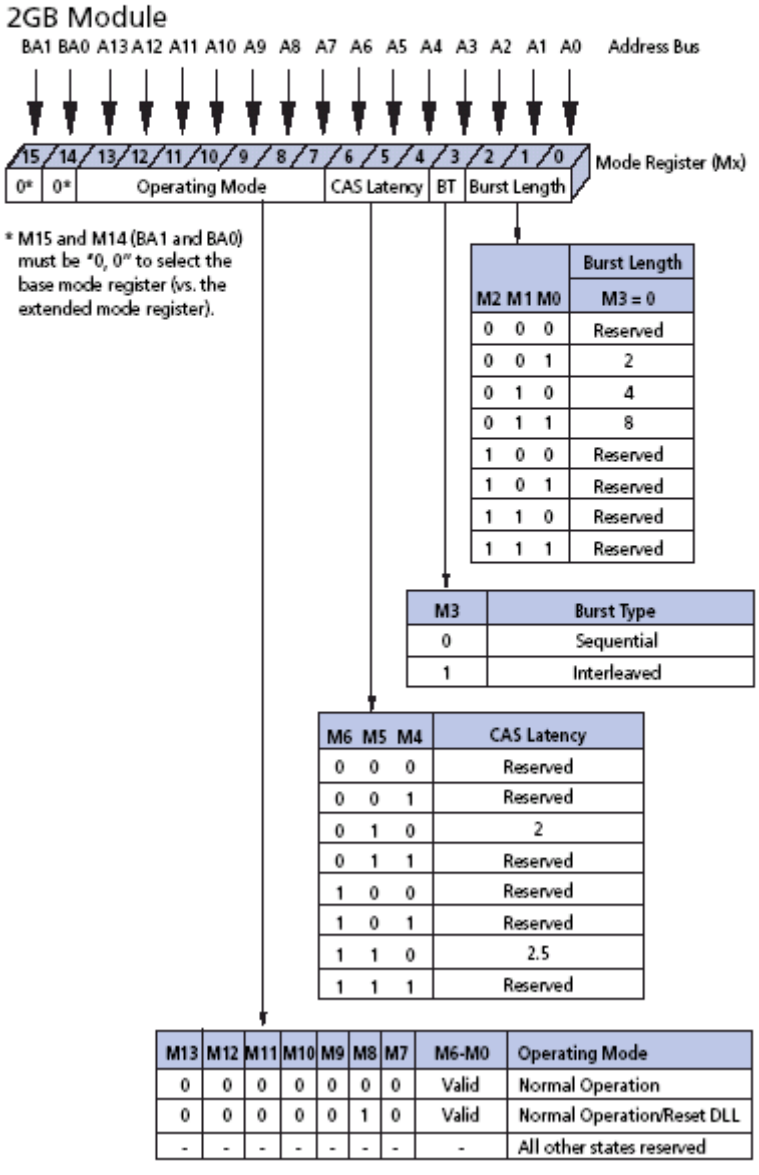
Mode Register Definition

The mode register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode. The mode register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Figure 5: Mode Register Definition Diagram





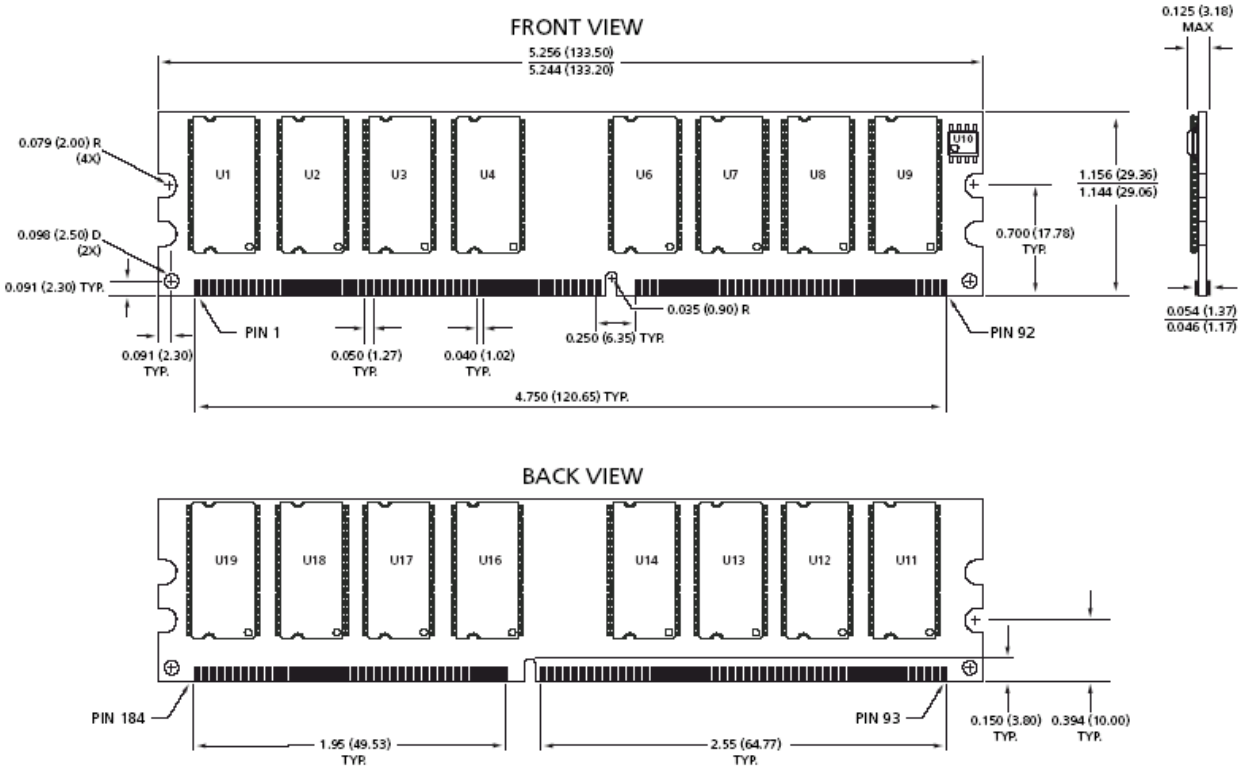
M2 M1 M0	Burst Length M3 = 0
0 0 0	Reserved
0 0 1	2
0 1 0	4
0 1 1	8
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	Reserved
1 0 0	Reserved
1 0 1	Reserved
1 1 0	2.5
1 1 1	Reserved

M13	M12	M11	M10	M9	M8	M7	M6-M0	Operating Mode
0	0	0	0	0	0	0	Valid	Normal Operation
0	0	0	0	0	1	0	Valid	Normal Operation/Reset DLL
-	-	-	-	-	-	-	-	All other states reserved

Figure 6: 184-Pin DIMM Dimensions – Low Profile



NOTE:

All dimensions arein inches (millimeters); $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

