DDR3 Registered/ECC Mini-DIMM Module

8GB based on 4Gbit (512Mx8) component

Revision 1.0 (September, 2012)
-Initial Release

1.0 Feature

- JEDEC standard V_{DDQ}=1.5V +/- 0.075V Power Supply
- VDDQ = 1.5V ± 0.075V
- Programmable CAS Latency: 6,7,8,9,10,11
- Programmable Additive Latency(Posted CAS) : 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency(CWL) = 5(DDR3-800), 6(DDR3-1066), 7(DDR3-1333) and 8(DDR3-1600)
- 400MHz fCK for 800Mb/sec/pin, 533MHz fCK for 1066Mb/sec/pin, 667MHz fCK for 1333Mb/sec/pin, 800MHz fCK for 1600Mb/sec/pin
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Internal (self) calibration: Internal self calibration through ZQ pin (RZQ: 240 ohm ± 1%)
- Bi-directional Differential Data Strobe
- Asynchronous Reset
- On-Die termination using ODT pin
- 8 independent internal bank
- Average Refresh Period 7.8us at lower than a TCASE 85°C, 3.9us at 85°C < TCASE < 95 °C
- Serial presence detect with EEPROM
- Mini-RDIMM Dimension (Nominal) 30.0 mm high, 82.0 mm wide
- Based on JEDEC standard reference Raw Cards Lay out.
- RoHS compliant
- Gold plated contacts

2.0 Ordering Information

Part number	Density	Module Organization	Component composition	Component PKG	Module Rank	Description
W16MB8G8x	8GB	1Gx72	512Mx8 x18pcs	FBGA	2	PC3-12800

Note: Last Character of the Part Number (x) representing DRAM vendor
S=Samsung; M=Micron; H=Hynix

3.0 Key Timing Parameters

	DDR3-1600	Unit
CL-tRCD-tRP	11-11-11	tCK
CAS Latency	11	tCK
tCK(min)	1.25	ns
tRCD(min)	13.5	ns
tRP(min)	13.5	ns
tRAS(min)	35	ns
tRC(min)	48.75	ns

4.0 Absolute Maximum DC Rating

Symbol	Parameter	Rating	Units
V_{in}, Vout	Voltage on any pin relative to V_{SS}	-0.4 ~ 1.975	V
V_{DD}	Voltage on V_{DD} & V_{DDQ} supply relative to V_{ss}	-0.4 ~ 1.975	V
V_{DDQ}	Short circuit current	-0.4 ~ 1.975	V
V_{DDL}	Power dissipation	-0.4 ~ 1.975	V
T_{STG}	Storage Temperature	-55 ~ + 100	°C

5.0 DIMM Pin Configurations (Front side/Back side)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VTT	31	DQ24	61	VDD	92	DQ40	123	VTT	153	DQ29	183	A3	214	DQ45
2	VREFDQ	32	DQ25	62	A2	93	DQ41	124	VSS	154	VSS	184	A1	215	VSS
3	VSS	33	VSS	63	VDD	94	VSS	125	DQ4	155	DM3/ TDQS12	185	VDD	216	DM5/ TDQS14
	DQ0	34	DQS3#	64	NC	95	DQS5#	126	DQ5	156	NF/ TDQS12#	186	CK0	217	NF/ TDQS14#
	DQ1	35	DQS3	65	NC	96	DQS5	127	VSS	157	VSS	187	CK0#	218	VSS
6	VSS	36	VSS	66	VDD	97	VSS	128	DM0/ TDQS9	158	DQ30	188	VDD	219	DQ46
7	DQS0#	37	DQ26	67	VREFCA	98	DQ42	129	NF/ TDQS9#	159	DQ31	189	VDD	220	DQ47
8	DQS0	38	DQ27	68	VDD	99	DQ43	130	VSS	160	VSS	190	EVENT#	221	VSS
9	VSS	39	VSS	69	Par_In	100	VSS	131	DQ6	161	CB4	191	A0	222	DQ52
10	DQ2	40	CB0	70	VDD	101	DQ48	132	DQ7	162	CB5	192	VDD	223	DQ53
11	DQ3	41	CB1	71	A10	102	DQ49	133	VSS	163	VSS	193	BA1	224	VSS
12	VSS	42	VSS	72	BA0	103	VSS	134	DQ12	164	DM8/ TDQS17	194	VDD	225	DM6/ TDQS15
13	DQ8	43	DQS8#	73	VDD	104	DQS6#	135	DQ13	165	NF/ TDQS17#	195	RAS#	226	NF/ TDQS15#
14	DQ9	44	DQS8	74	WE#	105	DQS6	136	VSS	166	VSS	196	CS0#	227	VSS
15	VSS	45	VSS	75	CAS#	106	VSS	137	DM1/ TDQS10	167	CB6	197	VDD	228	DQ54
16	DQS1#	46	CB2	76	VDD	107	DQ50	138	NF/ TDQS10#	168	CB7	198	ODT0	229	DQ55
17	DQS1	47	CB3	77	CS1#	108	DQ51	139	VSS	169	VSS	199	A13	230	VSS
18	VSS	48	VSS	78	ODT1	109	VSS	140	DQ14	170	NC	200	VDD	231	DQ60
19	DQ10	49	NC	79	VDD	110	DQ56	141	DQ15	171	NC	201	NC	232	DQ61
20	DQ11	50	RESET#	80	NC	111	DQ57	142	VSS	172	CKE1	202	NC	233	VSS
21	VSS	51	CKE0	81	NC	112	VSS	143	DQ20	173	VDD	203	VSS	234	DM7/ TDQS16
22	DQ16	52	VDD	82	VSS	113	DQS7#	144	DQ21	174	A15	204	DQ36	235	NF/ TDQS16#
23	DQ17	53	BA2	83	DQ32	114	DQS7	145	VSS	175	A14	205	DQ37	236	VSS
24	VSS	54	Err_Out#	84	DQ33	115	VSS	146	DM2/ TDQS11	176	VDD	206	VSS	237	DQ62
25	DQS2#	55	VDD	85	VSS	116	DQ58	147	NF/ TDQS11#	177	A12	207	DM4/ TDQS13	238	DQ63
26	DQS2	56	A11	86	DQS4#	117	DQ59	148	VSS	178	A9	208	NF/ TDQS13#	239	VSS
27	VSS	57	A7	87	DQS4	118	VSS	149	DQ22	179	VDD	209	VSS	240	VDDSPD
28	DQ18	58	VDD	88	VSS	119	SA0	150	DQ23	180	A8	210	DQ38	241	SA1
29	DQ19	59	A5	89	DQ34	120	SCL	151	VSS	181	A6	211	DQ39	242	SDA
30	VSS	60	A4	90	DQ35	121	SA2	152	DQ28	182	VDD	212	VSS	243	VSS
				91	VSS	122	VTT					213	DQ44	244	VTT

6.0 DIMM Pin Description

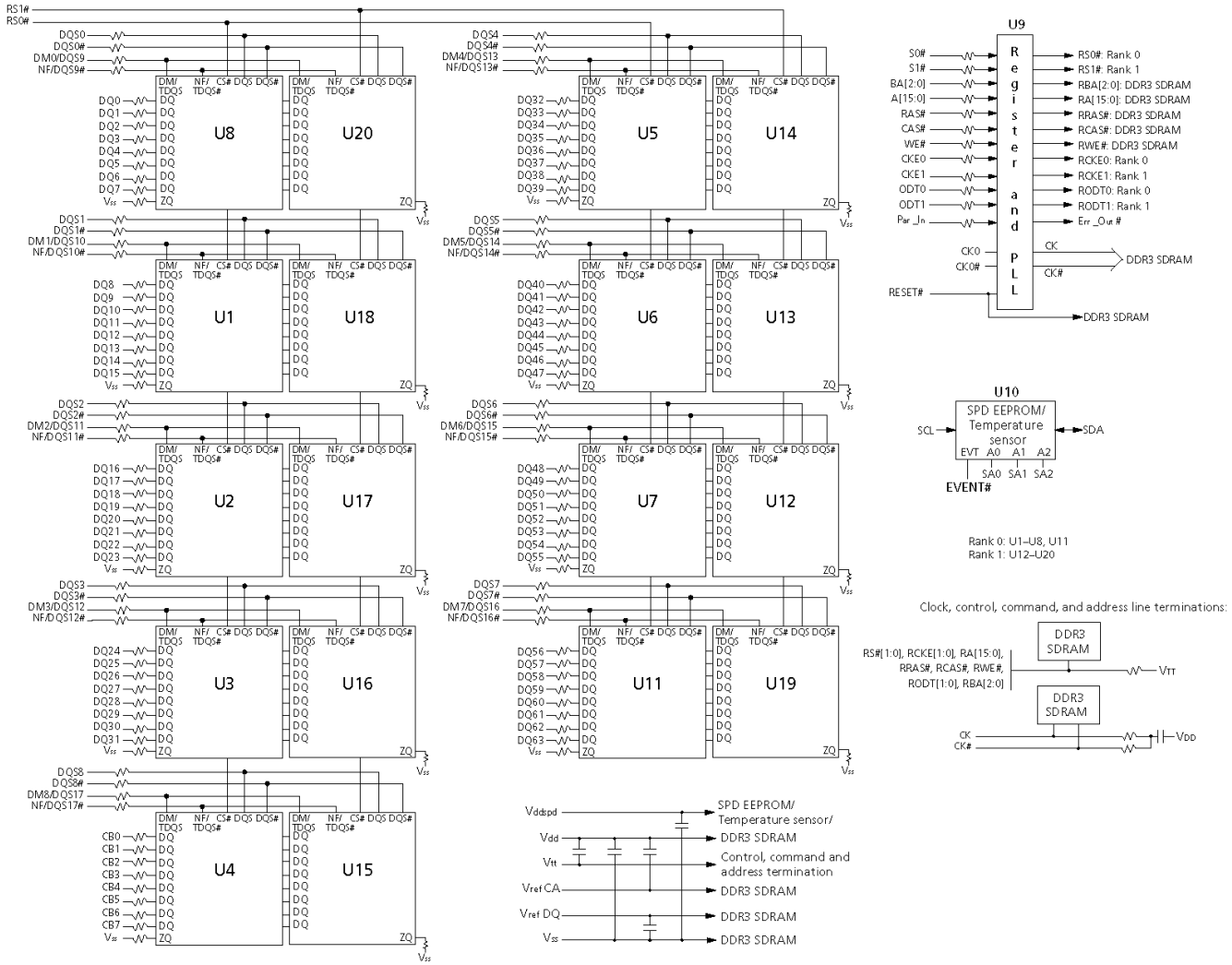
The pin description table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

Name	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments Table for density-specific addressing information.
BAx	Input	**Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command.
CKx, CKx#	Input	**Clock:** Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	**Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DMx	Input	**Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	**On-die termination:** Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for Ax, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW asychronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed.
Sx#	Input	**Chip select:** Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I_2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I_2C bus.
CBx	I/O	**Check bits:** Used for system error detection and correction.
DQx	I/O	**Data input/output:** Bidirectional data bus.
DQSx, DQSx#	I/O	**Data strobe:** Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-aligned with write data.
SDA	I/O	**Serial data:** Used to transfer addresses and data into and out of the temperature sen-sor/SPD EEPROM on the I_2C bus.
TDQSx, TDQSx#	Output	**Redundant data strobe (x8 devices only):** TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function.
Err_Out#	Output (open drain)	**Parity error output:** Parity error found on the command and address bus.
EVENT#	Output (open drain)	**Temperature event:**The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V. The component V_{DD} and V_{DDQ} are connected to the module V_{DD}.
V_{DDSPD}	Supply	**Temperature sensor/SPD EEPROM power supply:** 3.0–3.6V.
V_{REFCA}	Supply	**Reference voltage:** Control, command, and address $V_{DD}/2$.
V_{REFDQ}	Supply	**Reference voltage:** DQ, DM $V_{DD}/2$.
V_{SS}	Supply	Ground.
V_{TT}	Supply	**Termination voltage:** Used for control, command, and address $V_{DD}/2$.
NC	–	**No connect:** These pins are not connected on the module.
NF	–	**No function:** These pins are connected within the module, but provide no functionality.

7.0 Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Pre-charge
512Mx8(4Gb)base	A0-A15	A0-A9	BA0-BA2	A10

8.0 Functional Block Diagram: 8GB; 1Gx72 Module (Populated as 2 ranks of x8 SDRAM Module)



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

9.0 AC & DC Operating Conditions

Recommended operating conditions (Voltage referenced to Vss=0V, TA=0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	1.425	1.5	1.575	V
V_{DDQ}	Supply Voltage for Output	1.425	1.5	1.575	V
$V_{REF}DQ_{(DC)}$	I/O Reference Voltage (DQ)	$0.49*V_{DDQ}$	$0.50*V_{DDQ}$	$0.51*V_{DDQ}$	V
$V_{REF}CA_{(DC)}$	I/O Reference Voltage (CMD/Add)	$0.49*V_{DDQ}$	$0.50*V_{DDQ}$	$0.51*V_{DDQ}$	V
V_{TT}	Termination Voltage	$0.49*V_{DDQ}$	$0.50*V_{DDQ}$	$0.51*V_{DDQ}$	V

10.0 Capacitance (Max.)

Symbol	Parameter/Condition	Min	Max	Unit
CCK	Input capacitance, CK and $\overline{CK}$	-	11	pF
CI1	Input capacitance, CKE and $\overline{CS}$	-	12	pF
CI2	Input capacitance, Addr, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	-	12	pF
CIO	Input capacitance, DQ, DM, DQS, $\overline{DQS}$	-	10	pF

11.1 AC Timing Parameters & Specifications

(AC operating conditions unless otherwise noted)

Parameter	Symbol	DDR3-1600		Units
		min	max	
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	ns
Average Clock Period	tCK(avg)	-		
Clock Period	tCK(abs)	tCK(avg) min +tJIT (per)min	tCK(avg) max +tJIT (per)max	ps
Average high pulse width	tCH(avg)	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	tCK(avg)
Clock Period Jitter	tJIT(per)	-70	70	ps
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-60	60	ps
Cycle to Cycle Period Jitter	tJIT(cc)	140	-	ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	120	-	ps
Cumulative error across 2 cycles	tERR(2per)	- 103	103	ps
Cumulative error across 3 cycles	tERR(3per)	- 122	122	ps
Cumulative error across 4 cycles	tERR(4per)	- 136	136	ps
Cumulative error across 5 cycles	tERR(5per)	- 147	147	ps
Cumulative error across 6 cycles	tERR(6per)	- 155	155	ps
Cumulative error across 7 cycles	tERR(7per)	- 163	163	ps
Cumulative error across 8 cycles	tERR(8per)	- 169	169	ps
Cumulative error across 9 cycles	tERR(9per)	- 175	175	ps
Cumulative error across 10 cycles	tERR(10per)	- 180	180	ps

11.2 AC Timing Parameters & Specifications (cont.)

Parameter	Symbol	DDR3-1600		Units
		min	max	
Cumulative error across 11 cycles	tERR(11per)	- 184	184	ps
Cumulative error across 12 cycles	tERR(12per)	- 188	188	ps
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 = 0.68ln(n))*tJIT(per)max		ps
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	tCK(avg)
Absolute clock Low pulse width	tCL(abs)	0.43	-	tCK(avg)
Data Timing				
DQS, /DQS to DQ skew, per group, per access	tDQSQ	-	100	ps
DQ output hold time from DQS, /DQS	tQH	0.38	-	tCK(avg)
DQ low-impedance time from CK, /CK	tLZ(DQ)	-450	225	ps
DQ high-impedance time from CK, /CK	tHZ(DQ)	-	225	ps
Data setup time to DQS, /DQS referenced to Vih(ac)Vil(ac) levels	tDS(base) AC175	TBD	-	ps
	tDS(base) AC150	10	-	ps
Data hold time to DQS, /DQS referenced to Vih(ac)Vil(ac) levels	tDH(base) DC100	45	-	ps
DQ and DM Input pulse width for each input	tDIPW	360	-	ps
Data Strobe Timing				
DQS, /DQS READ Preamble	tRPRE	0.9	-	tCK
DQS, /DQS differential READ Postamble	tRPST	0.3	-	tCK
DQS, /DQS output high time	tQSH	0.4	-	tCK(avg)
DQS, /DQS output low time	tQSL	0.4	-	tCK(avg)
DQS, /DQS WRITE Preamble	tWPRE	0.9	-	tCK
DQS, /DQS WRITE Postamble	tWPST	0.3	-	tCK
DQS, /DQS rising edge output access time from rising CK, /CK	tDQSCK	-225	225	ps
DQS, /DQS low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	ps
DQS, /DQS high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	ps
DQS, DQS differential input low pulse width	tDQSL	0.45	0.55	tCK
DQS, DQS differential input high pulse width	tDQSH	0.45	0.55	tCK
DQS, DQS rising edge to CK, /CK rising edge	tDQSS	-0.27	0.27	tCK(avg)
DQS,DQS faling edge setup time to CK, /CK rising edge	tDSS	0.18	-	tCK(avg)
DQS,DQS faling edge hold time to CK, /CK rising edge	tDSH	0.18	-	tCK(avg)
DLL locking time	tDLLK	512	-	nCK
internal READ Command to PRECHARGE Command delay	tRTP	max (4tCK,7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max (4tCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	nCK
Mode Register Set command update delay	tMOD	max (12tCK,15ns)	-	
CAS# to CAS# command delay	tCCD	4	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(AVG))		nCK

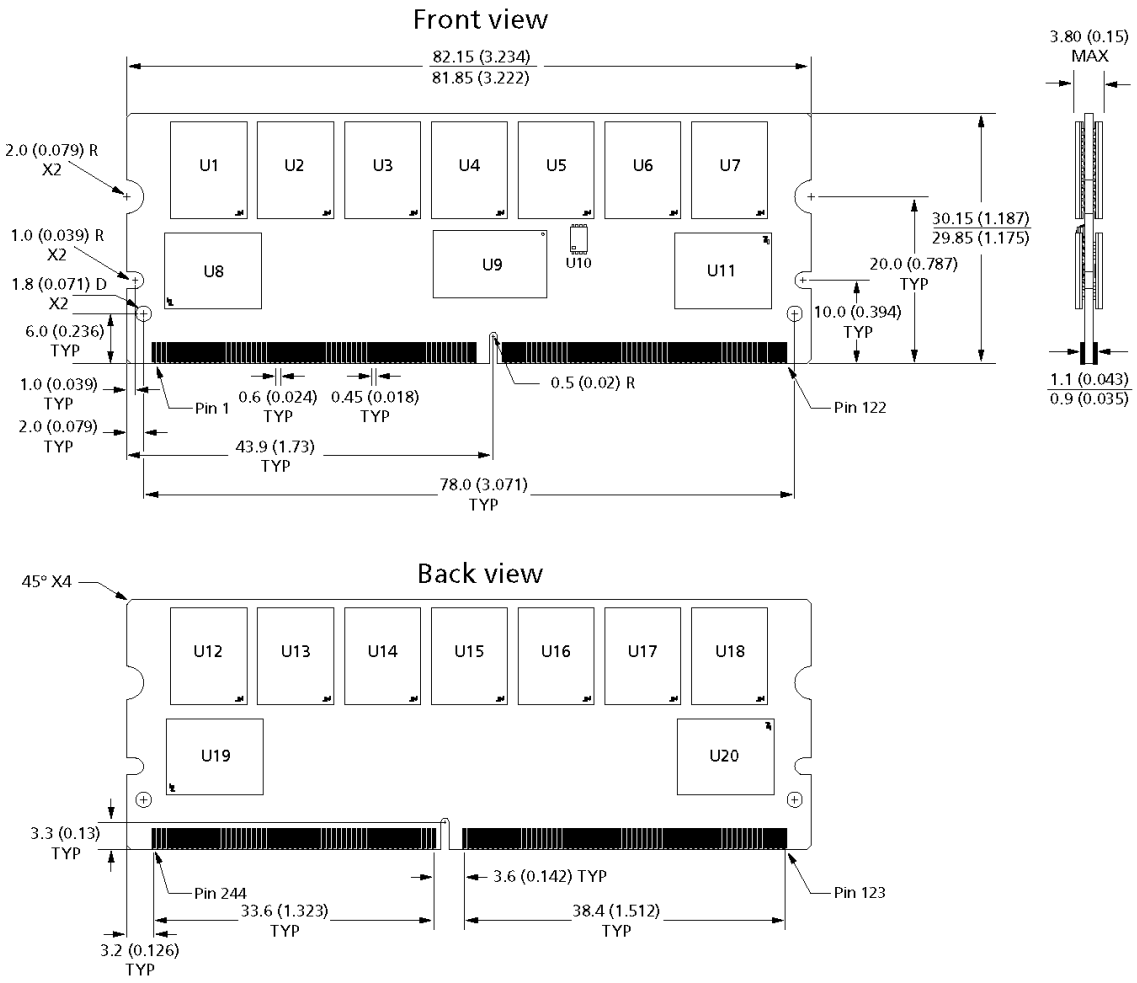
11.3 AC Timing Parameters & Specifications (cont.)

Parameter	Symbol	DDR3-1600		Units
		min	max	
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK
ACTIVE to PRECHARGE command period	tRAS	36	70,000	ns
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4tCK,6ns)	-	
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4tCK,7.5ns)	-	
Four activate window for 1KB page size	tFAW	30	-	ns
Four activate window for 2KB page size	tFAW	40	-	ns
Command and Address setup time to CK, /CK referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC175	45	-	ps
	tIS(base) AC150	45+125	-	ps
Command and Address hold time from CK, /CK referenced to Vih(ac) / Vil(ac) levels	tIH(base) DC100	120	-	ps
Control & Address Input pulse width for each input	tIPW	560	-	ps
Calibration Timing				
Power-up and RESET calibration time	tZQinitI	512	-	tCK
Normal operation Full calibration time	tZQoper	256	-	tCK
Normal operation short calibration time	tZQCS	64	-	tCK
Reset Timing				
Exit Reset from CKE HIGH to a valid command	tXPR	max(5tCK, tRFC+ 10ns)	-	
Self Refresh Timing				
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5tCK,tRFC+ 10ns)	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	nCK
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE)	tCKSRE	max(5tCK, 10ns)	-	
Valid Clock Requirement before Self Refresh Exit (SRX)	tCKSRX	max(5tCK, 10ns)	-	
Power Down Timing				
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (3tCK,6ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max(10tCK, 24ns)	-	
CKE minimum pulse width	tCKE	max(3tCK, 5 ns)	-	
Command pass disable delay	tCPDED	1	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCK
Timing of ACT command to Power Down entry	tACTPDEN	1	-	nCK
Timing of PRE command to Power Down entry	tPRPDEN	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 +1	-	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRPDEN	WL + 4 +(tWR/tCK)	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN	WL + 4 +WR+1	-	nCK
Timing of WR command to Power Down entry (BL4MRS)	tWRPDEN	WL + 2 +(tWR/ tCK(avg))	-	nCK

11.4 AC Timing Parameters & Specifications (cont.)

Parameter	Symbol	DDR3-1600		Units
		min	max	
Timing of WRA command to Power Down entry (BL4MRS)	tWRAPDEN	WL +2 +WR +1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	1	-	
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	
ODT Timing				
ODT high time without write command or with wirte commandand BC4	ODTH4	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	nCK
Asynchronous RTT tum-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	ns
Asynchronous RTT tum-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	ns
ODT turn-on	tAON	-225	225	ps
RTT_NOM and RTT_WR turn-off time from ODTL off reference	tAOF	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)
Write Leveling Timing				
First DQS pulse rising edge after tDQSS margining mode is programmed	tWLMRD	40	-	tCK
DQS/DQS delay after tDQS margining mode is programmed	tWLDQSEN	25	-	tCK
Setup time for tDQSS latch	tWLS	165	-	ps
Hold time of tDQSS latch	tWLH	165	-	ps
Write leveling output delay	tWLO	0	7.5	ns
Write leveling output error	tWLOE	0	2	ns

12.0 Physical Dimensions: 1Gx72 (2 Ranks) (512Mx8 Based)



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.