DDR2 VLP-Registered DIMM Module

256MB based on 256Mbit component

512MB, 1GB based on 512Mbit component

1GB, 2GB, 4GB based on 1Gbit component

ATCA Compliant

60 Balls FBGA with Pb-Free

Revision 1.0 (Mar. 2006)
-Initial Release

1.0 Feature

- JEDEC standard 1.8V +/- 0.1V Power Supply
- 240-pin, very low profile mini dual in-line memory module (VLP DIMM)
- ATCA compliant
- Fast data transfer rates: PC2-3200, PC2-4200, or PC2-5300
- Supports ECC error detection and correction
- 256MB (32M x 72), 512MB (64M x 72), 1GB (128M x 72), 2GB(256M x 72), 4GB(512M x 72)
- VDD = VDDQ = +1.8V
- VDDSPD = +1.7V to +3.6V
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency (WL) = READ latency (RL) - 1 tCK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence detect (SPD) with EEPROM
- Gold edge contacts

2.0 Ordering Information

Part number	Density	Module Organization	Component composition	Component PKG	Module Rank	Description
S56TV8AMX	256MB	32Mx72	32Mx8*9	FBGA	1	256MB 1Rx8 PC2-5300R-555
S56TV8AJX	256MB	32Mx72	32Mx8*9	FBGA	1	256MB 1Rx8 PC2-4200R-444
S56TV8AHX	256MB	32Mx72	32Mx8*9	FBGA	1	256MB 1Rx8 PC2-3200R-333
S12TV8BMX	512MB	64Mx72	64Mx8*9	FBGA	1	512MB 1Rx8 PC2-5300R-555
S12TV8BJX	512MB	64Mx72	64Mx8*9	FBGA	1	512MB 1Rx8 PC2-4200R-444
S12TV8BHX	512MB	64Mx72	64Mx8*9	FBGA	1	512MB 1Rx8 PC2-3200R-333
S1GTV8CMX	1GB	128Mx72	128Mx8*9	FBGA	1	1GB 1Rx8 PC2-5300R-555
S1GTV8CJX	1GB	128Mx72	128Mx8*9	FBGA	1	1GB 1Rx8 PC2-4200R-444
S1GTV8CHX	1GB	128Mx72	128Mx8*9	FBGA	1	1GB 1Rx8 PC2-3200R-333
S1GTV4AMX	1GB	128Mx72	128Mx4*18	FBGA	1	1GB 1Rx8 PC2-5300R-555
S1GTV4AJX	1GB	128Mx72	128Mx4*18	FBGA	1	1GB 1Rx8 PC2-4200R-444
S1GTV4AHX	1GB	128Mx72	128Mx4*18	FBGA	1	1GB 1Rx8 PC2-3200R-333
S2GTV4DMX	2GB	256Mx72	256Mx4*18	FBGA	1	2GB 1Rx4 PC2-5300R-555
S2GTV4DJX	2GB	256Mx72	256Mx4*18	FBGA	1	2GB 1Rx4 PC2-4200R-444
S2GTV4DHX	2GB	256Mx72	256Mx4*18	FBGA	1	2GB 1Rx4 PC2-3200R-333
S2GTV4BMX	2GB	256Mx72	256Mx4(st)*18	FBGA	2	2GB 2Rx4 PC2-5300R-555
S2GTV4BJX	2GB	256Mx72	256Mx4(st)*18	FBGA	2	2GB 2Rx4 PC2-4200R-444
S2GTV4BHX	2GB	256Mx72	256Mx4(st)*18	FBGA	2	2GB 2Rx4 PC2-3200R-333
S4GTV4CMX	4GB	512Mx72	512Mx4(st)*18	FBGA	2	4GB 2Rx4 PC2-5300R-555
S4GTV4CJX	4GB	512Mx72	512Mx4(st)*18	FBGA	2	4GB 2Rx4 PC2-4200R-444
S4GTV4CHX	4GB	512Mx72	512Mx4(st)*18	FBGA	2	4GB 2Rx4 PC2-3200R-333

Note: Last Character x of the Part Number stand for DRAM vendor
S=Samsung; M=Micron; Q=Qimonda; H=Hynix; E=Elpida

3.0 Operating Frequencies

	DDR2-667	DDR2-533	DDR-400	Unit
Speed @ CL3	400	400	400	Mbps
Speed @ CL4	533	533	400	Mbps
Speed @ CL5	667	-	-	Mbps
CL-tRCD-tRP	5-5-5	4-4-4	3-3-3	CK

4.0 Absolute Maximum DC Rating

Symbol	Parameter		Rating	Units
$V_{in,}$ Vout	Voltage on any pin relative to V_{SS}		-0.5 ~ 2.3	V
V_{DD}	Voltage on V_{DD} & V_{DDQ} supply relative to V_{ss}		-1.0 ~ 2.3	V
V_{DDQ}	Short circuit current		-0.5 ~ 2.3	V
V_{DDL}	Power dissipation		-0.5 ~ 2.3	V
T_{STG}	Storage Temperature		-55 ~ + 100	°C
Tcase	DDR2 SDRAM device operating temperature (ambient)		0~85	°C
TOPR	Operating temperature (ambient)		0~55	°C
I_I	Input leakage current; Any input 0V ≤ VIN ≤ VDD; VREF input 0V ≤ VIN ≤0.95V; (All other pins not under test=0V)	Command/Address, RAS#, CAS#, WE# S#, CKE, CK, CK#, DM	-5~5	µA
I_{OZ}	Output leakage current; 0V ≤ VOUT ≤ VDDQ; DQs and ODT are disabled	DQ, DQS, DQS#	-5~5	µA
I_{VREF}	VREF leakage current; VREF = Valid VREF level		-18~18	µA

5.0 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back	Pin	Back
1	V_{REF}	31	DQ19	61	A4	91	VSS	121	VSS	151	VSS	181	VDDQ	211	DM5/DQS14
2	VSS	32	VSS	62	VDDQ	92	DQS5#	122	DQ4	152	DQ28	182	A3	212	NC/DQS14#
3	DQ0	33	DQ24	63	A2	93	DQS5	123	DQ5	153	DQ29	183	A1	213	VSS
4	DQ1	34	DQ25	64	VDD	94	VSS	124	VSS	154	VSS	184	VDD	214	DQ46
5	VSS	35	VSS	65	VSS	95	DQ42	125	DM0/DQS9	155	DM3/DQS12	185	CK0	215	DQ47
6	DQS0#	36	DQS3#	66	VSS	96	DQ43	126	NC/DQS9#	156	NC/DQS12#	186	CK0#	216	VSS
7	DQS0	37	DQS3	67	VDD	97	VSS	127	VSS	157	VSS	187	VDD	217	DQ52
8	VSS	38	VSS	68	Par_in	98	DQ48	128	DQ6	158	DQ30	188	A0	218	DQ53
9	DQ2	39	DQ26	69	VDD	99	DQ49	129	DQ7	159	DQ31	189	VDD	219	VSS
10	DQ3	40	DQ27	70	A10/AP	100	VSS	130	VSS	160	VSS	190	BA1	220	RFU
11	VSS	41	VSS	71	BA0	101	SA2	131	DQ12	161	CB4	191	VDDQ	221	RFU
12	DQ8	42	CB0	72	VDDQ	102	NC	132	DQ13	162	CB5	192	RAS#	222	VSS
13	DQ9	43	CB1	73	WE#	103	VSS	133	VSS	163	VSS	193	S0#	223	DM6/DQS15
14	VSS	44	VSS	74	CAS#	104	DQS6#	134	DM1/DQS10	164	DM8/DQS17	194	VDDQ	224	NC/DQS15#
15	DQS1#	45	DQS8#	75	VDDQ	105	DQS6	135	NC/DQS10#	165	NC/DQS17#	195	ODT0	225	VSS
16	DQS1	46	DQS8	76	NC	106	VSS	136	VSS	166	VSS	196	NC/A13	226	DQ54
17	VSS	47	VSS	77	NC	107	DQ50	137	RFU	167	CB6	197	VDD	227	DQ55
18	Reset#	48	CB2	78	VDDQ	108	DQ51	138	RFU	168	CB7	198	VSS	228	VSS
19	NC	49	CB3	79	VSS	109	VSS	139	VSS	169	VSS	199	DQ36	229	DQ60
20	VSS	50	VSS	80	DQ32	110	DQ56	140	DQ14	170	VDDQ	200	DQ37	230	DQ61
21	DQ10	51	VDDQ	81	DQ33	111	DQ57	141	DQ15	171	NC	201	VSS	231	VSS
22	DQ11	52	CKE0	82	VSS	112	VSS	142	VSS	172	VDD	202	DM4/DQS13	232	DM7/DQS16
23	VSS	53	VDD	83	DQS4#	113	DQS7#	143	DQ20	173	NC	203	NC/RQS13#	233	NC/DQS16#
24	DQ16	54	NC/BA2	84	DQS4	114	DQS7	144	DQ21	174	NC	204	VSS	234	VSS
25	DQ17	55	Err_Out	85	VSS	115	VSS	145	VSS	175	VDDQ	205	DQ38	235	DQ62
26	VSS	56	VDDQ	86	DQ34	116	DQ58	146	DM2/DQS11	176	A12	206	DQ39	236	DQ63
27	DQS2#	57	A11	87	DQ35	117	DQ59	147	NC/DQS11#	177	A9	207	VSS	237	VSS
28	DQS2	58	A7	88	VSS	118	VSS	148	VSS	178	VDD	208	DQ44	238	VDDSPD
29	VSS	59	VDD	89	DQ40	119	SDA	149	DQ22	179	A8	209	DQ45	239	SA0
30	DQ18	60	A5	90	DQ41	120	SCL	150	DQ23	180	A6	210	VSS	240	SA1

Note: Pin 196 is NC for 256MB or A13 for 512MB and 1GB; pin 54 is NC for 256MB and 512MB, or BA2 for 1GB

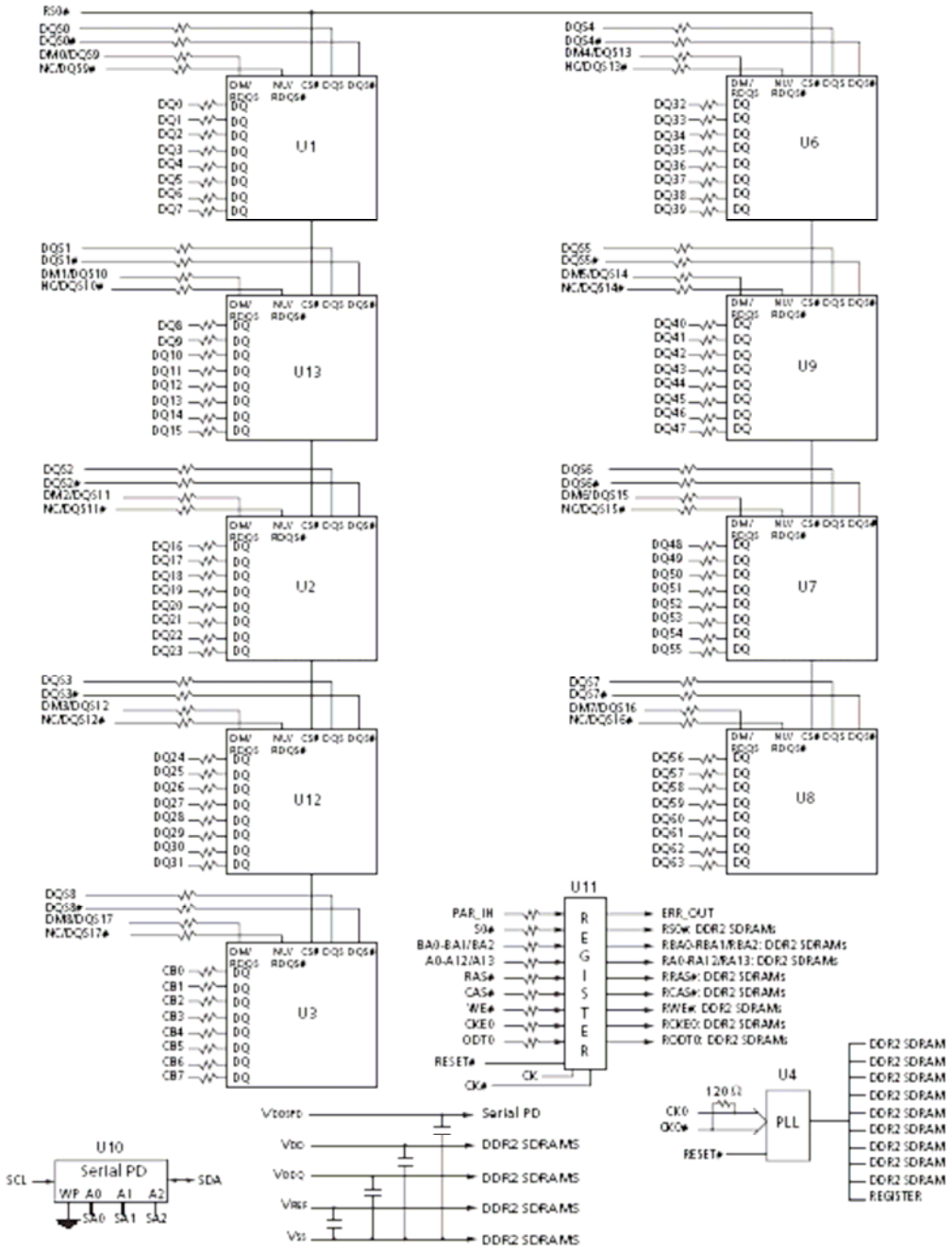
6.0 DIMM Pin Description

Pin Name	Function	Pin Name	Function
A0 ~ A12 (256MB), A0 ~ A13 (512MB, 1GB)	Address input (Multiplexed)	ODT0	On Die Termination
A10/AP	Address Input/Auto precharge	CB0~CB7	Data check bits Input/Output
BA0, BA1, BA2 (1GB)	Bank Select	DQ0~DQ63	Data Input/Output
CK0 ~ CK0#	Clock input	DQS0~DQS8 DQS0# ~ DQS17#	Data strobes, negative line
CKE0	Clock enable input	DM (0~8), DQS (9~17)	Data Masks/Data strobes (Read)
S0#	Chip select input	Reset#	Register and PLL control pin
RAS#	Row address strobe	RFU	Reserved for future used
CAS#	Column address strobe	NC	No connection
WE#	Write Enable	V_{DD}	Core Power
SCL	SPD Clock Input	V_{DDQ}	I/O Power
SDA	SPD Data Input/Output	V_{SS}	Ground
SA0~SA2	SPD Address	V_{REF}	Input/Output Reference
Par_In	Parity bit for address & Control bus	V_{DDSPD}	SPD
Err_Out	Parity error found in the Address and Control bus		

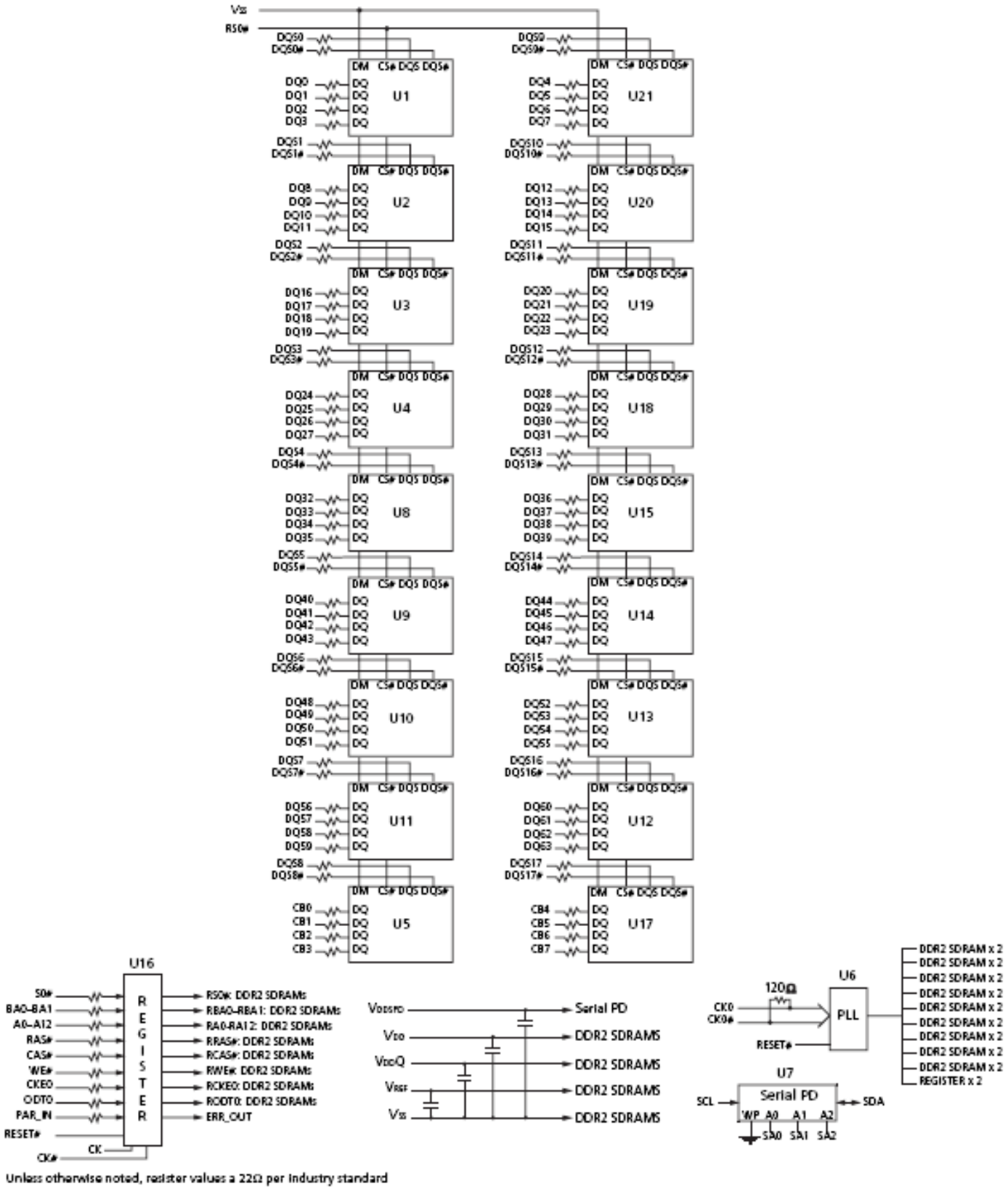
7.0 Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
128Mx8(1Gb) base	A0-A13	A0-A9	BA0-BA2	A10
64Mx8(512Mb) base	A0-A13	A0-A9	BA0-BA1	A10
32Mx8(256Mb) base	A0-A12	A0-A9	BA0-BA1	A10

8.1 Functional Block Diagram: 256MB, 512MB, 1GB Module (Populated as 1 rank of x8 SDRAM Module)

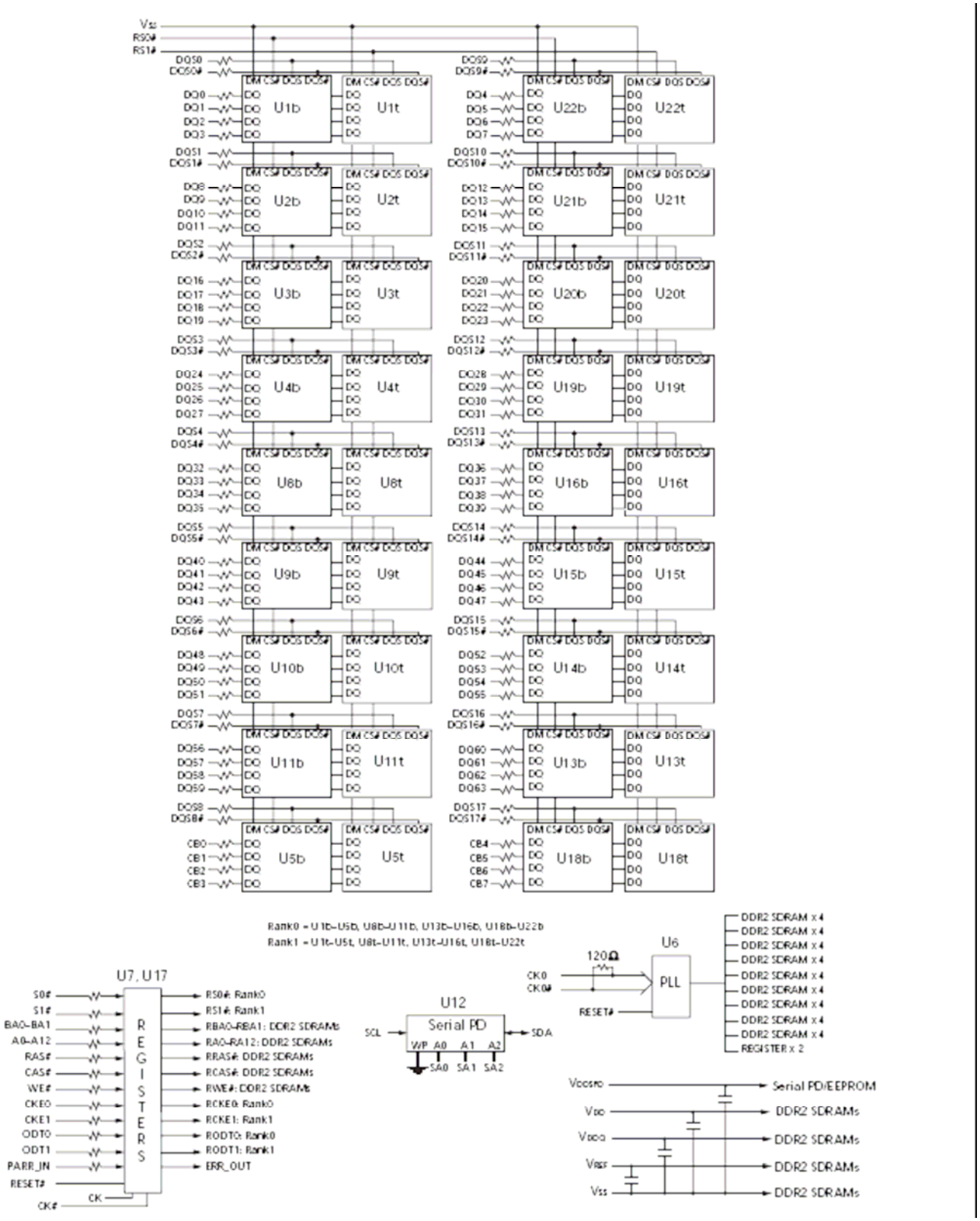


8.1 Functional Block Diagram: 1GB/2GB Module (Populated as 1 rank of x4 SDRAM Module)



Unless otherwise noted, resister values a 22Ω per Industry standard

8.3 Functional Block Diagram: 2GB/4GB Module (Populated as 2 rank of 256Mbx4 stack/512Mbx4 stack SDRAM Module)



9.0 AC & DC Operating Conditions

Recommended operating conditions (Voltage referenced to Vss=0V, TA=0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	1.7	1.8	1.9	V
V_{DDL}	Supply Voltage for DLL	1.7	1.8	1.9	V
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V
V_{REF}	Input Reference Voltage	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	mV
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V

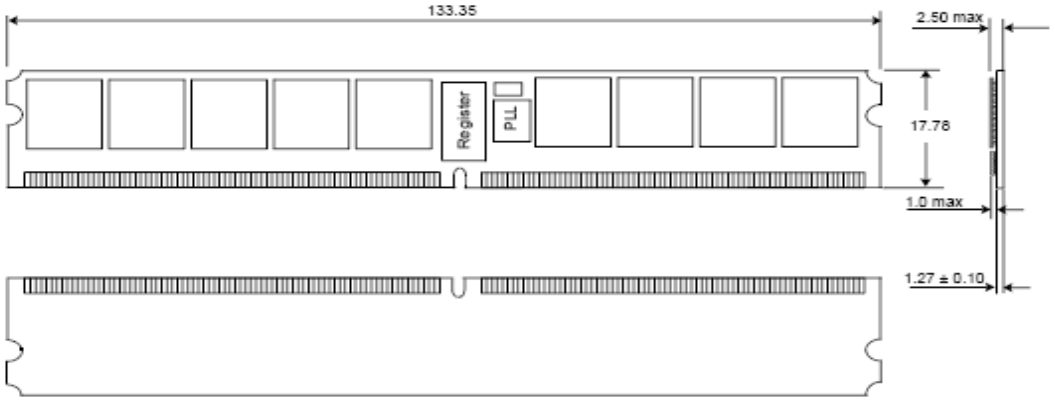
10.0 AC Timing Parameters & Specifications

(AC operating conditions unless otherwise noted)

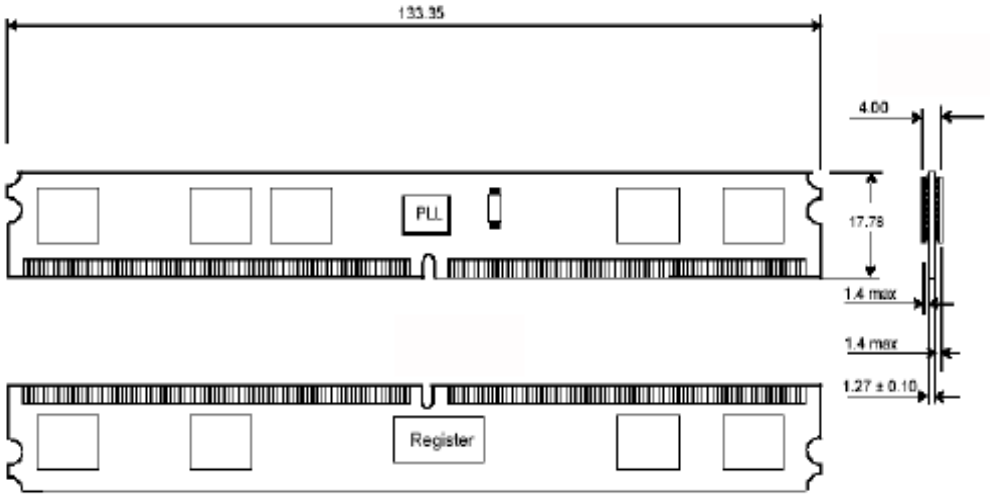
Parameter	Symbol	DDR2-667		DDR2-533		DDR2-400		Units
		min	max	min	max	min	max	
DQ output access time from CK/$\overline{CK}$	tAC	-450	+450	-500	+500	-600	+600	ps
DQS output access time from CK/$\overline{CK}$	tDQSCK	-400	+400	-450	+450	-500	+500	ps
CK high-level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK
CK low-level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK
CK half period	tHP	min(tCL, tCH	x	min(tCL, tCH	x	min(tCL, tCH	x	ps
Clock cycle time, CL=x	tCK	3000	8000	3750	8000	5000	8000	ps
DQ and DM input hold time	tDH(base)	175	x	225	x	275	x	ps
DQ and DM input setup time	tDS(base)	100	x	100	x	150	x	ps
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	0.6	x	tCK
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	0.35	x	tCK
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	x	tAC max	x	tAC max	ps
DQS low-impedance time from CK/$\overline{CK}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	tAC min	tAC max	ps
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2*tAC min	tAC max	2*tAC min	tAC max	2*tAC min	tAC max	ps
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	240	x	300	x	350	ps
DQ hold skew factor	tQHS	x	340	x	400	x	450	ps
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	tHP - tQHS	x	ps
First DQS latching transition to associated clock edge	tDQSS	-0.25	0.25	-0.25	0.25	-0.25	0.25	tCK
DQS input high pulse width	tDQSH	0.35	x	0.35	x	0.35	x	tCK
DQS input low pulse width	tDQSL	0.35	x	0.35	x	0.35	x	tCK
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	0.2	x	tCK
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	0.2	x	tCK
Mode register set command cycle timet	tMRD	2	x	2	x	2	x	tCK
Write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Write preamble	tWPRE	0.35	x	0.35	x	0.35	x	tCK
Address and control input hold time	tIH(base)	275	x	375	x	475	x	ps
Address and control input setup time	tIS(base)	200	x	250	x	350	x	ps

Parameter	Symbol	DDR2-667		DDR2-533		DDR2-400		Units
		min	max	min	max	min	max	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Active to active command period for 1KB page size products	tRRD	7.5	x	7.5	x	7.5	x	ns
Active to active command period for 2KB page size products	tRRD	10	x	10	x	10	x	ns
Four Activate Window for 1KB page size productst	tFAW	37.5		37.5		37.5		ns
Four Activate Window for 2KB page size products	tFAW	50		50		50		ns
CAS to CAS command delay	tCCD	2		2		2		tCK
Write recovery time	tWR	15	x	15	x	15	x	ns
Auto precharge write recovery + precharge time	tDAL	WR+tRP	x	WR+tRP	x	WR+tRP	x	tCK
Internal write to read command delay	tWTR	7.5	x	7.5	x	10	x	ns
Internal read to precharge command delay	tRTP	7.5		7.5		7.5		ns
Exit self refresh to a non-read command	tXSNRt	tRFC + 10		tRFC + 10		tRFC + 10		ns
Exit self refresh to a read command	tXSRD	200		200		200		tCK
Exit precharge power down to any non-read command	tXP	2	x	2	x	2	x	tCK
Exit active power down to read command	tXARD	2	x	2	x	2	x	tCK
Exit active power down to read command(slow exit, lower power)	tXARDS	7 - AL		6 - AL		6 - AL		tCK
CKE minimum pulse width(high and low pulse width)	tCKE	3		3		3		tCK
ODT turn-on delay	tAOND	2	2	2	2	2	2	tCK
ODT turn-on	tAON	tAC(min)	tAC(max)+0.7	tAC(min)	tAC(max)+1t	tAC(min)	tAC(max)+1t	ns
ODT turn-on(Power-Down mode)	tAONPD	tAC(min)+2	2tCK+ tAC(max)+1	tAC(min)+2	2tCK+ tAC(max)+1	tAC(min)+2	2tCK+ tAC(max)+1	ns
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	2.5	2.5	tCK
ODT turn-off	tAOF	tAC(min)	tAC(max)+ 0.6	tAC(min)	tAC(max)+ 0.6	tAC(min)	tAC(max)+ 0.6	ns
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5tCK +tAC(max)+1	tAC(min)+2	2.5tCK +tAC(max)+1	tAC(min)+2	2.5tCK +tAC(max)+1	ns
ODT to power down entry latency	tANPD	3		3		3		tCK
ODT power down exit latency	tAXPD	8		8		8		tCK
OCD drive mode output delay	tOIT	0	12	0	12	0	12	ns
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK +tIH		tIS+tCK +tIH		tIS+tCK +tIH		ns

11.1 Physical Dimensions: (32Mb/64Mb/128Mbx8 based)
256MB/512MB/1GB Module (1 Rank)

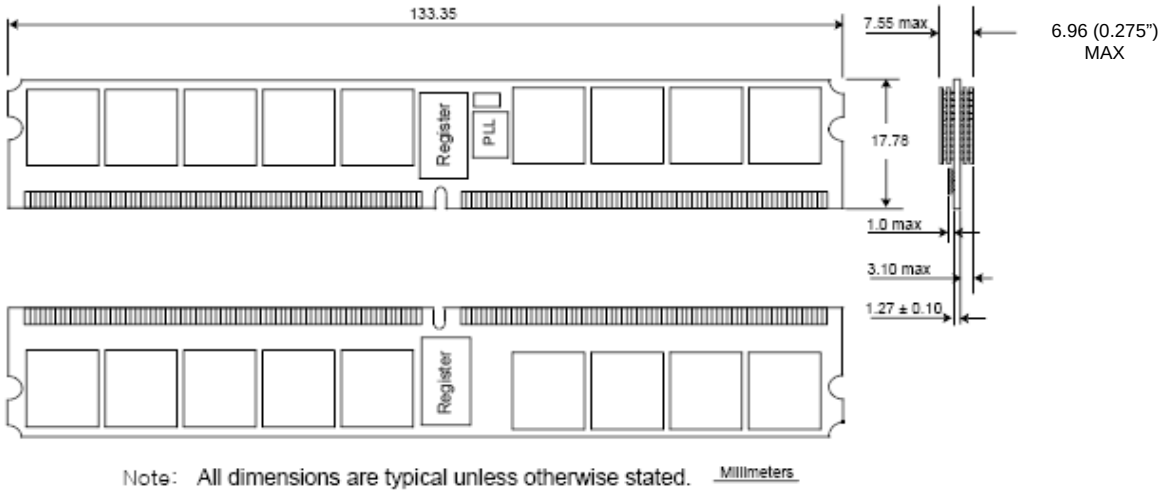


Note: All dimensions are typical unless otherwise stated. Millimeters



All dimensions are typical unless otherwise stated. Millimeters.

11.2 Physical Dimensions: (st.256Mbx4/ st.512Mbx4 based)
2GB/4GB Module (2 Rank)



Note: All dimensions are typical unless otherwise stated. Millimeters